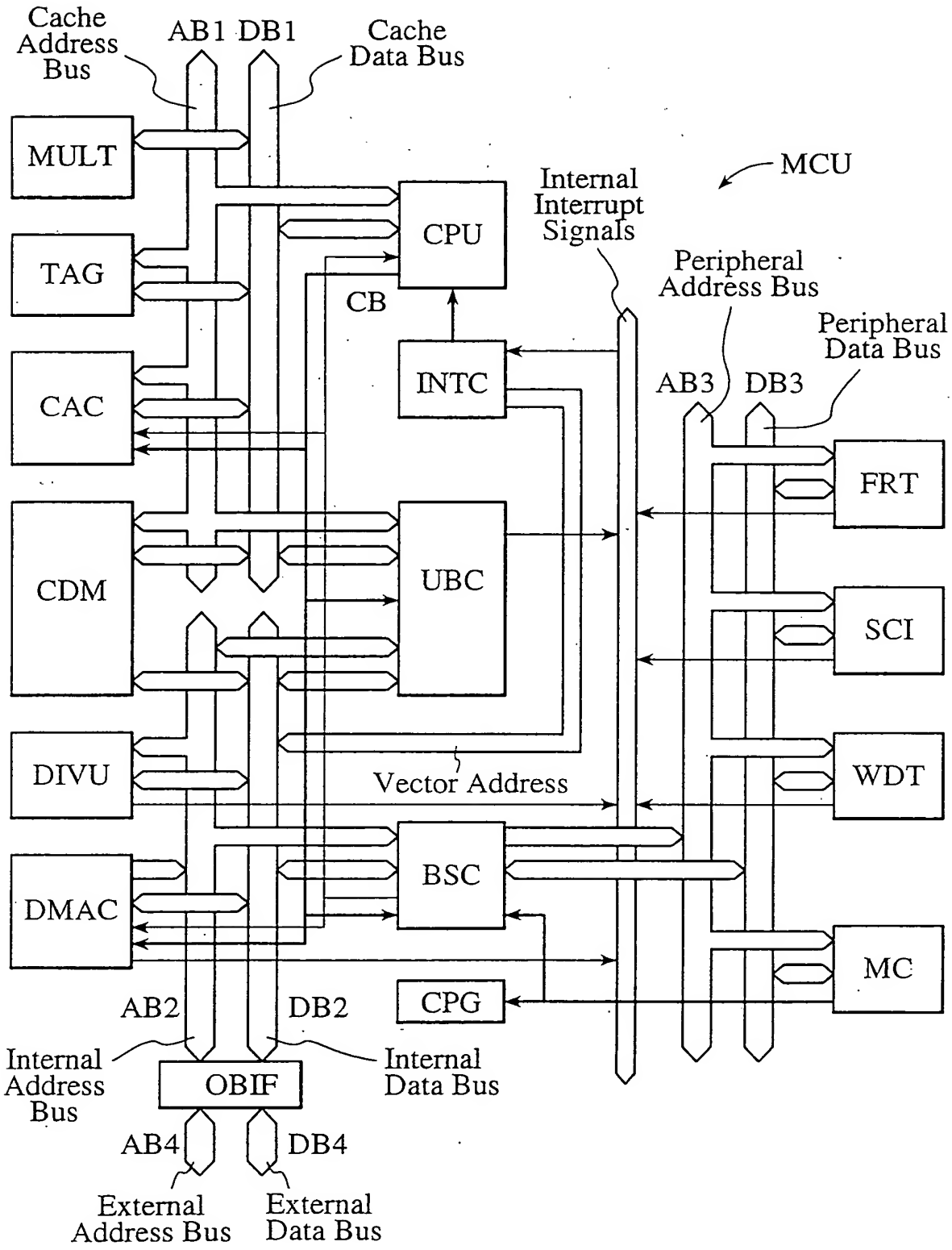

Cache Address Bus
AB1
DB1
Cache Data Bus
MULT
TAG
CAC
CDM
DIVU
DMAC
CPU
CB
INTC
UBC
BSC
CPG
MCU
Internal Interrupt Signals
Peripheral Address Bus
Peripheral Data Bus
AB3
DB3
FRT
SCI
WDT
MC
Vector Address
AB2
DB2
Internal Address Bus
Internal Data Bus
OBIF
AB4
DB4
External Address Bus
External Data Bus

FIG. 1

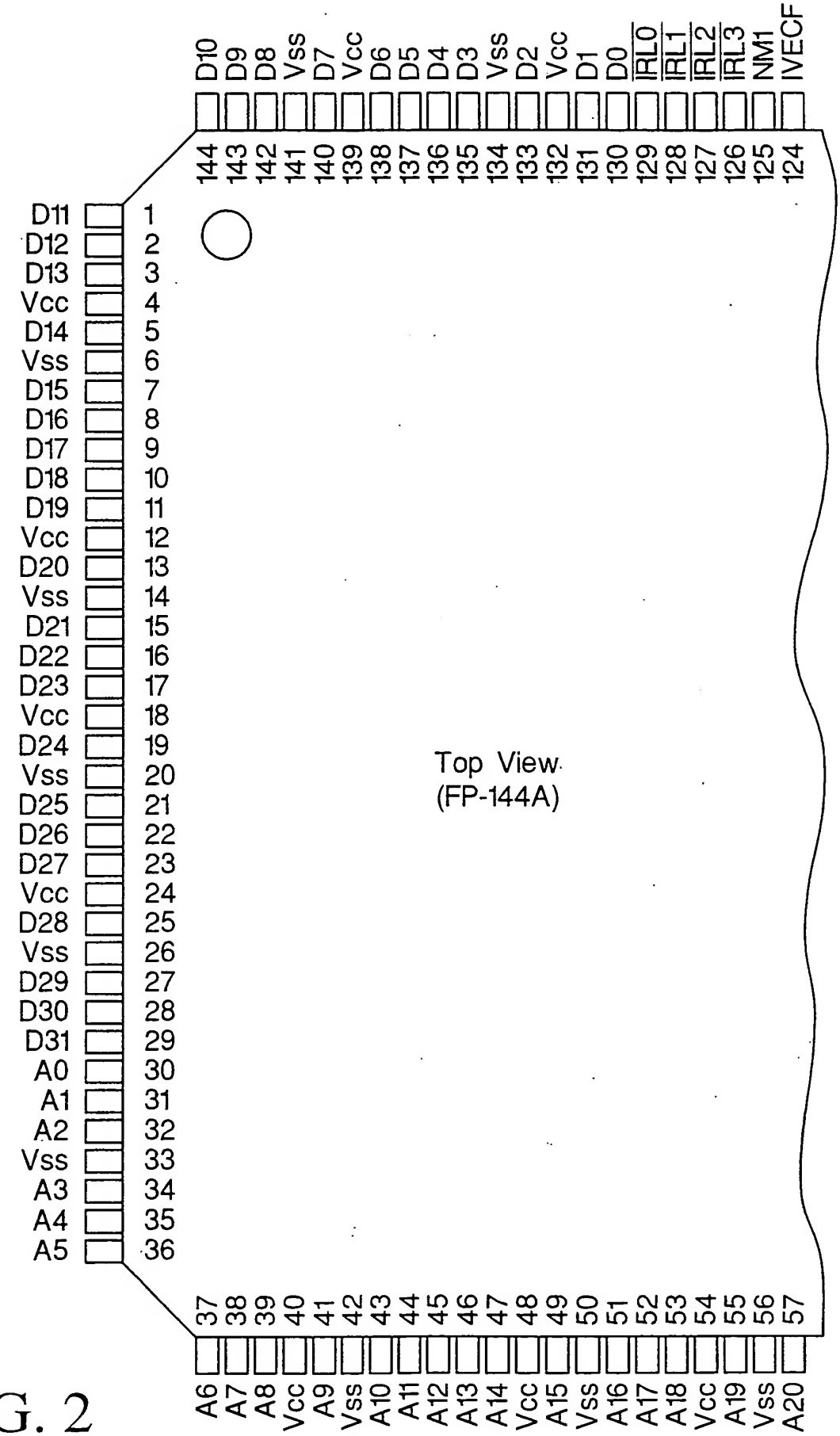

D10 144
D9 143
D8 142
Vss 141
D7 140
Vcc 139
D6 138
D5 137
D4 136
D3 135
Vss 134
D2 133
Vcc 132
D1 131
D0 130
IRL0 129
IRL1 128
IRL2 127
IRL3 126
NM1 125
IVECF 124
D11 1
D12 2
D13 3
Vcc 4
D14 5
Vss 6
D15 7
D16 8
D17 9
D18 10
D19 11
Vcc 12
D20 13
Vss 14
D21 15
D22 16
D23 17
Vcc 18
D24 19
Vss 20
D25 21
D26 22
D27 23
Vcc 24
D28 25
Vss 26
D29 27
D30 28
D31 29
A0 30
A1 31
A2 32
Vss 33
A3 34
A4 35
A5 36
Top View
(FP-144A)
37 A6
38 A7
39 A8
40 Vcc
41 A9
42 Vss
43 A10
44 A11
45 A12
46 A13
47 A14
48 Vcc
49 A15
50 Vss
51 A16
52 A17
53 A18
54 Vcc
55 A19
56 Vss
57 A20

FIG. 2

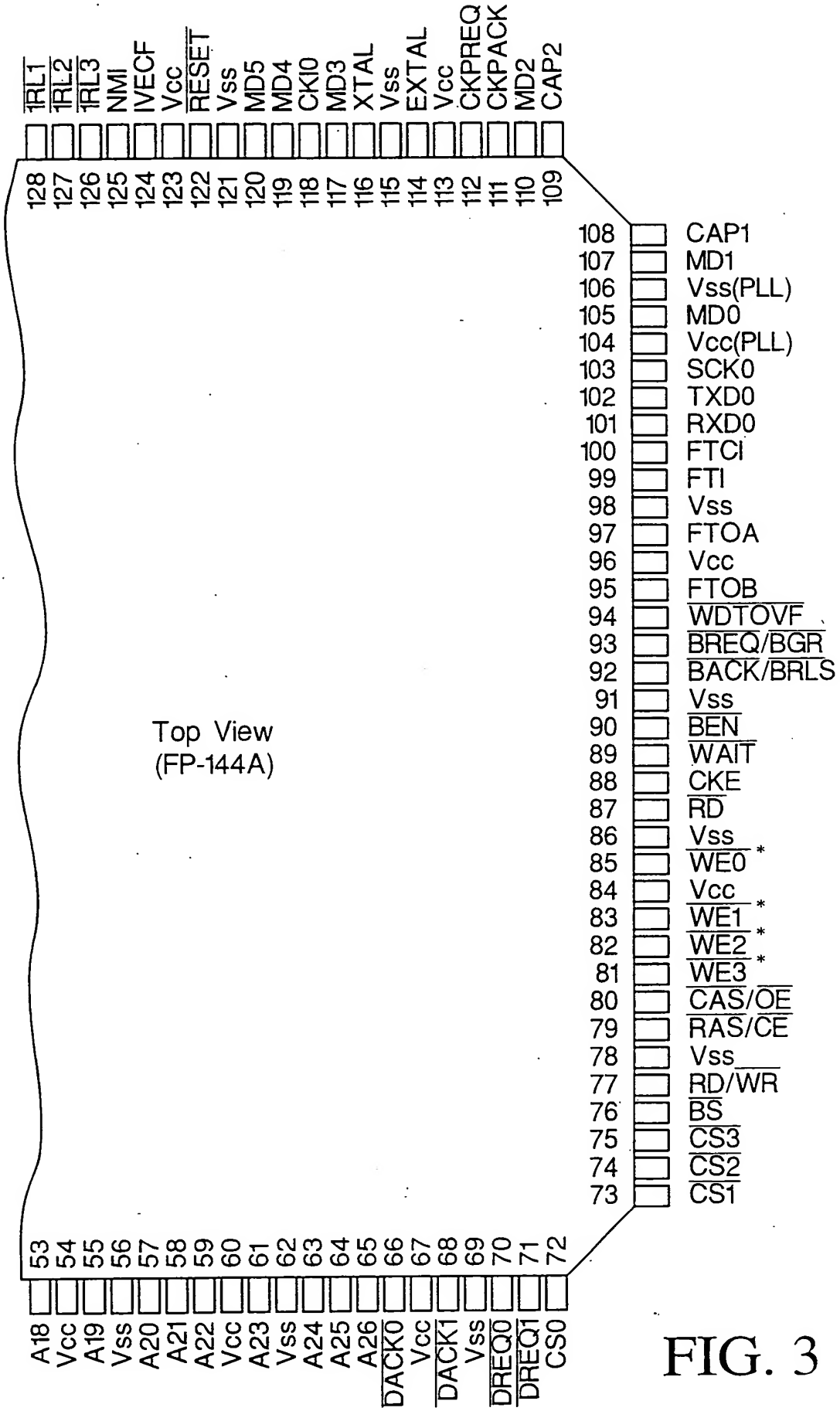

1RL1
1RL2
1RL3
NMI
IVECF
Vcc
RESET
Vss
MD5
MD4
CKIO
MD3
XTAL
Vss
EXTAL
Vcc
CKPREQ
CKPACK
MD2
CAP2
128 127 126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 110 109
108 CAP1
107 MD1
106 Vss(PLL)
105 MD0
104 Vcc(PLL)
103 SCK0
102 TXD0
101 RXD0
100 FTCI
99 FTI
98 Vss
97 FTOA
96 Vcc
95 FTOB
94 WDTOVF
93 BREQ/BGR
92 BACK/BRLS
91 Vss
90 BEN
89 WAIT
88 CKE
87 RD
86 Vss
85 WE0 *
84 Vcc
83 WE1 *
82 WE2 *
81 WE3 *
80 CAS/OE
79 RAS/CE
78 Vss
77 RD/WR
76 BS
75 CS3
74 CS2
73 CS1
Top View
(FP-144A)
53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72
A18 Vcc A19 Vss A20 A21 A22 Vcc A23 Vss A24 A25 A26 DACK0 Vcc DACK1 Vss DREQ0 DREQ1 CS0

FIG. 3

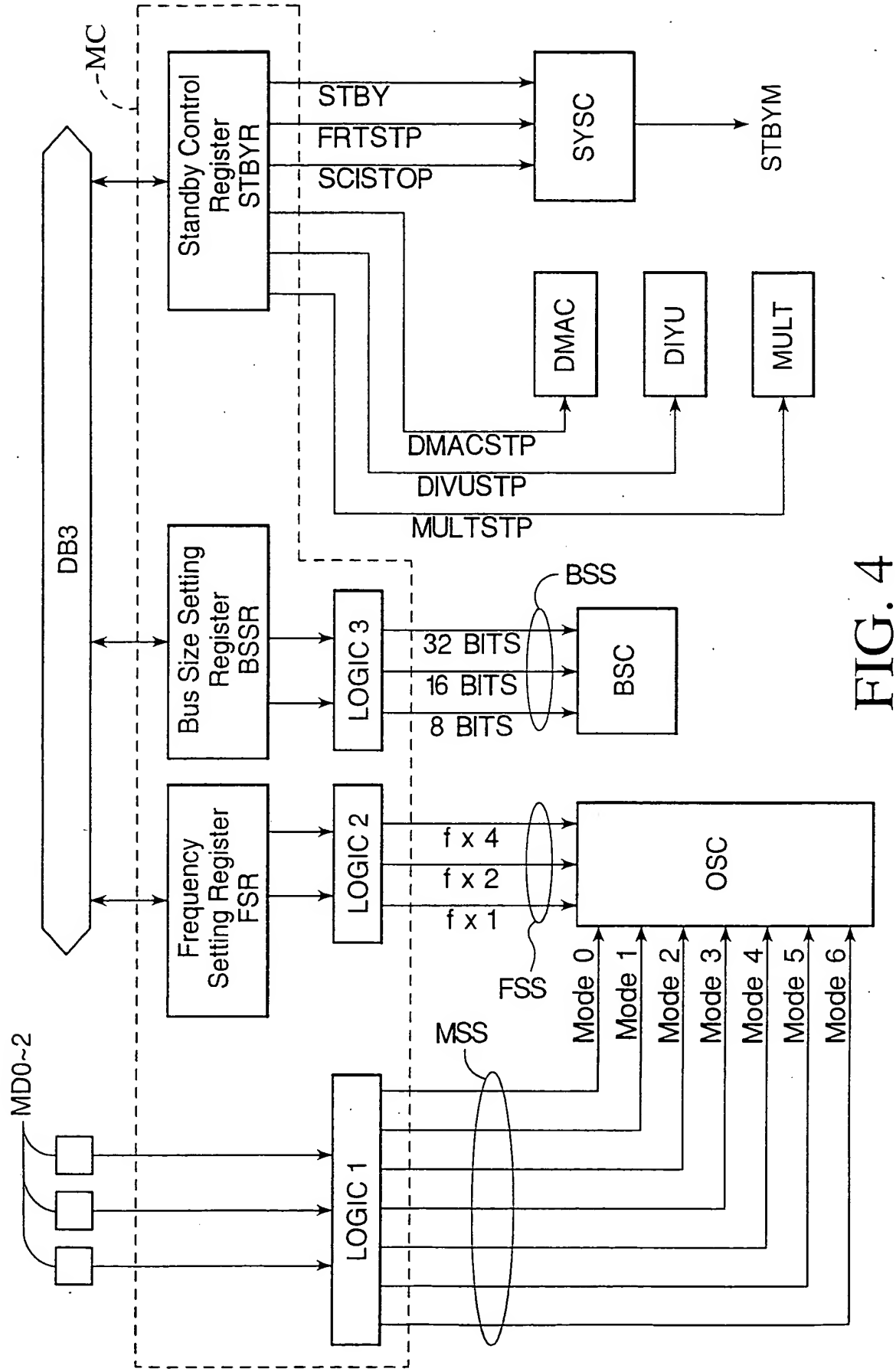

MC
Standby Control Register STBYR
STBY
FRTSTP
SCISTOP
SYSC
STBYM
DMAC
DIYU
MULT
DMACSTP
DIVUSTP
MULTSTP
DB3
Bus Size Setting Register BSSR
LOGIC 3
BSS
32 BITS
16 BITS
8 BITS
BSC
Frequency Setting Register FSR
LOGIC 2
f x 4
f x 2
f x 1
FSS
OSC
Mode 0
Mode 1
Mode 2
Mode 3
Mode 4
Mode 5
Mode 6
MSS
MD0~2
LOGIC 1

FIG. 4

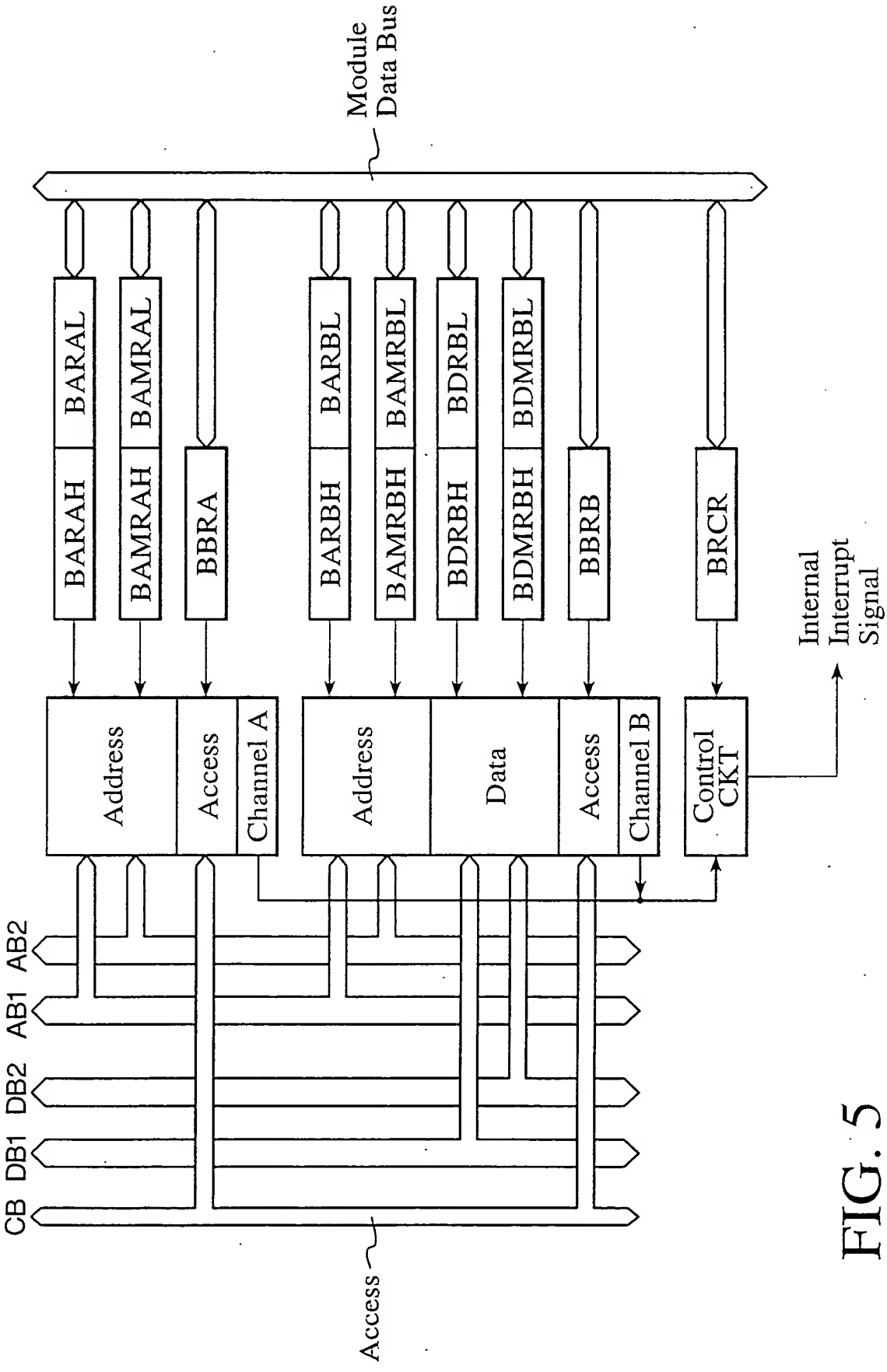
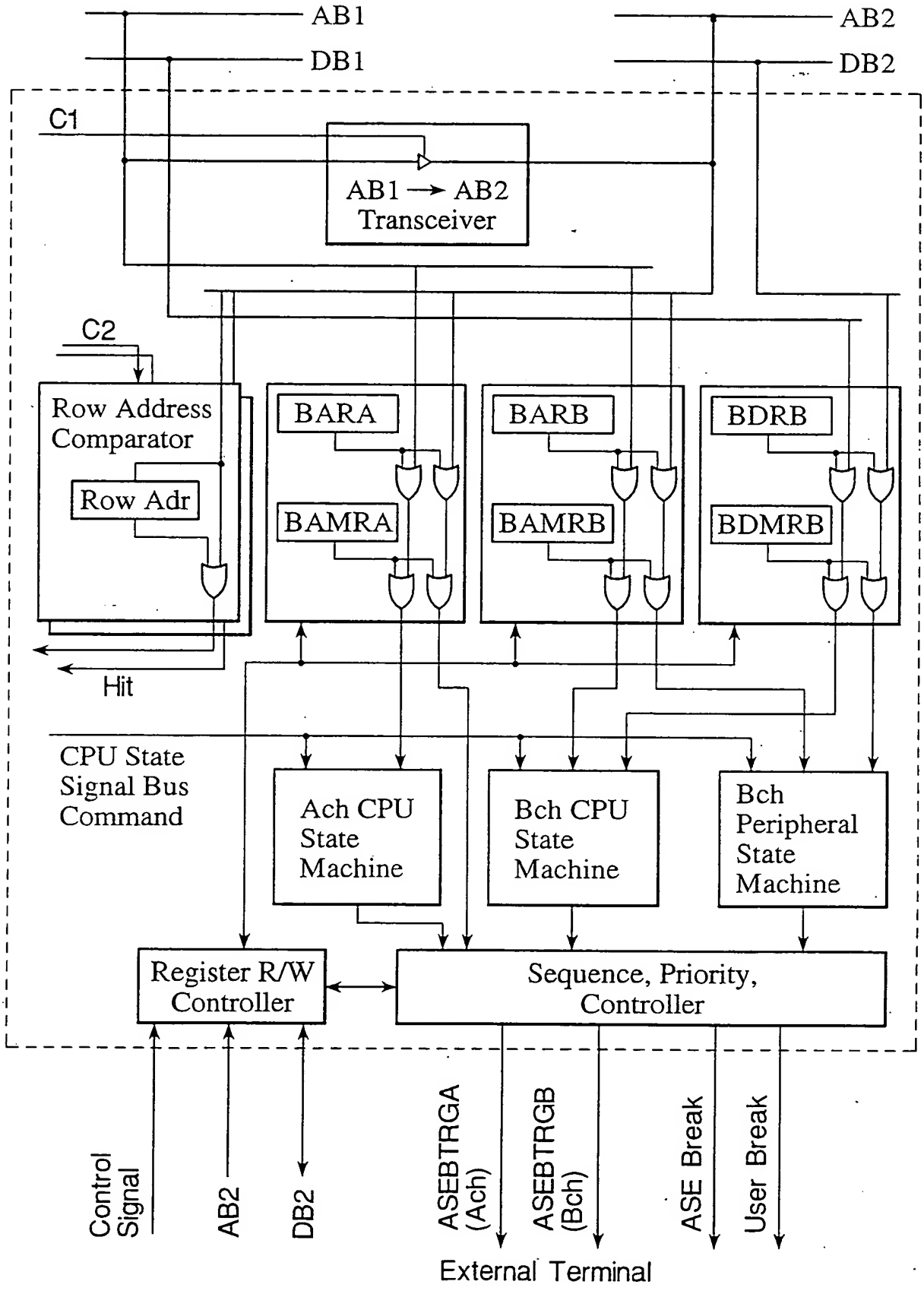

Module Data Bus
BARAL
BARAH
BAMRAL
BAMRAH
BBRA
BARBL
BARBH
BAMRBL
BAMRBH
BDRBL
BDRBH
BDMRBL
BDMRBH
BBRB
BRCR
Address
Access
Channel A
Address
Data
Access
Channel B
Control CKT
Internal Interrupt Signal
AB2
AB1
DB2
DB1
CB
Access

FIG. 5

FIG. 6


AB1
DB1
AB2
DB2
C1
AB1 → AB2
Transceiver
C2
Row Address
Comparator
Row Adr
BARA
BAMRA
BARB
BAMRB
BDRB
BDMRB
Hit
CPU State
Signal Bus
Command
Ach CPU
State
Machine
Bch CPU
State
Machine
Bch
Peripheral
State
Machine
Register R/W
Controller
Sequence, Priority,
Controller
Control
Signal
AB2
DB2
ASEBTRGA
(Ach)
ASEBTRGB
(Bch)
ASE Break
User Break
External Terminal

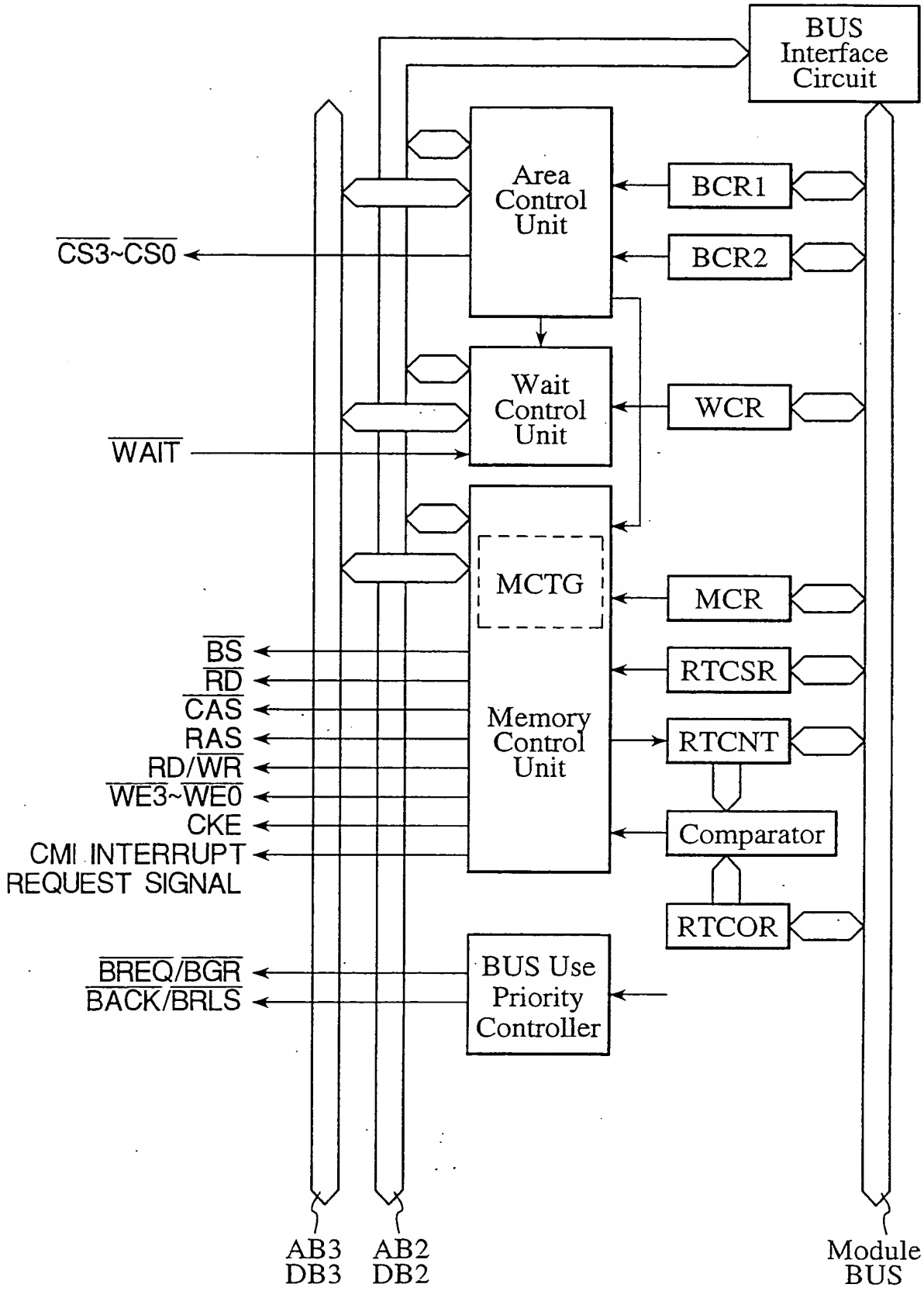

BUS Interface Circuit
Area Control Unit
BCR1
BCR2
CS3~CS0
Wait Control Unit
WCR
WAIT
MCTG
MCR
BS
RD
CAS
RAS
RD/WR
WE3~WE0
CKE
CMI INTERRUPT REQUEST SIGNAL
Memory Control Unit
RTCSR
RTCNT
Comparator
RTCOR
BREQ/BGR
BACK/BRLS
BUS Use Priority Controller
AB3
DB3
AB2
DB2
Module BUS

FIG. 7

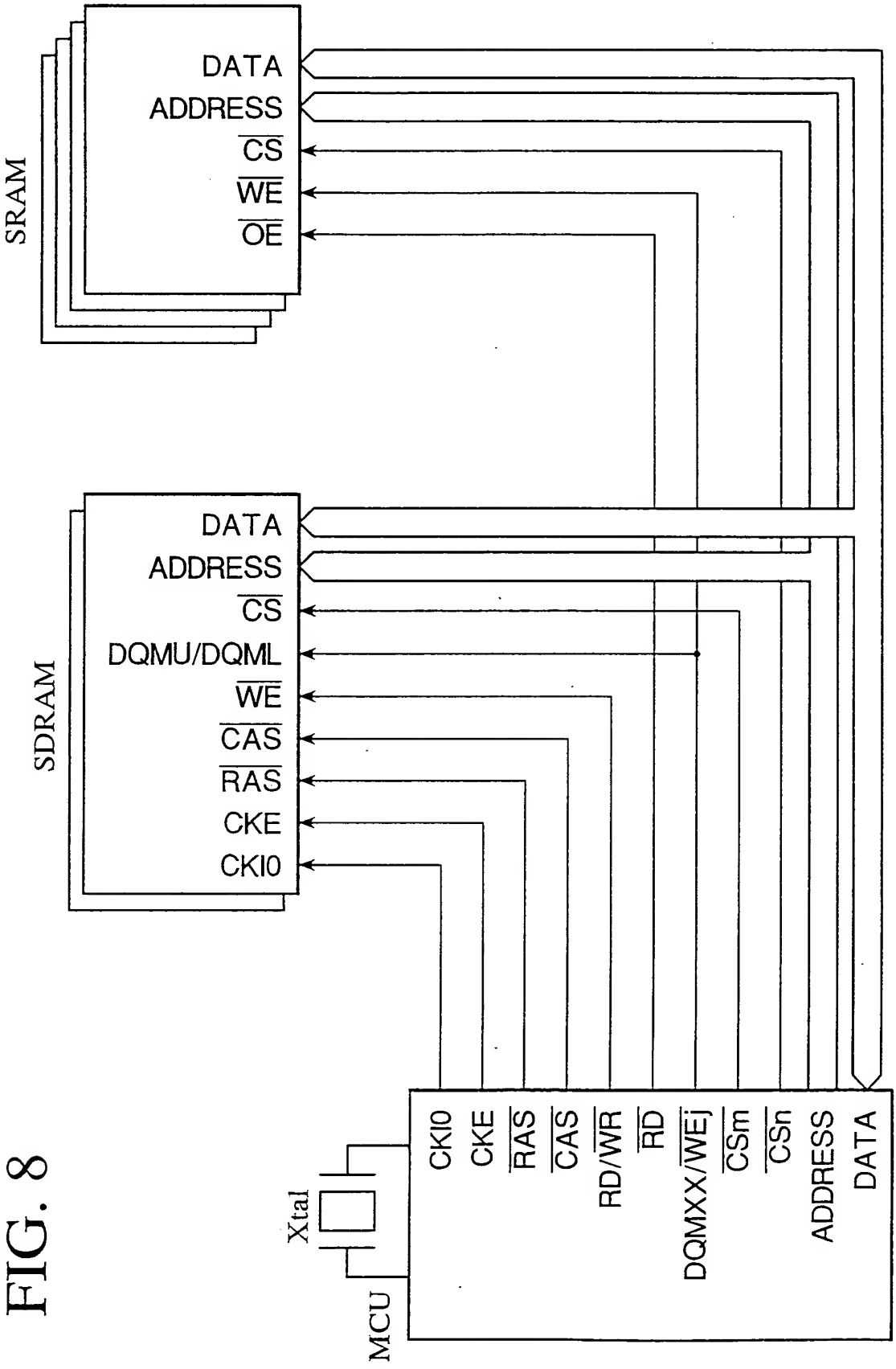

SRAM
DATA
ADDRESS
CS
WE
OE
SDRAM
DATA
ADDRESS
CS
DQMU/DQML
WE
CAS
RAS
CKE
CKI0
Xtal
MCU
CKI0
CKE
RAS
CAS
RD/WR
RD
DQMXX/WEj
CSm
CSn
ADDRESS
DATA

FIG. 8

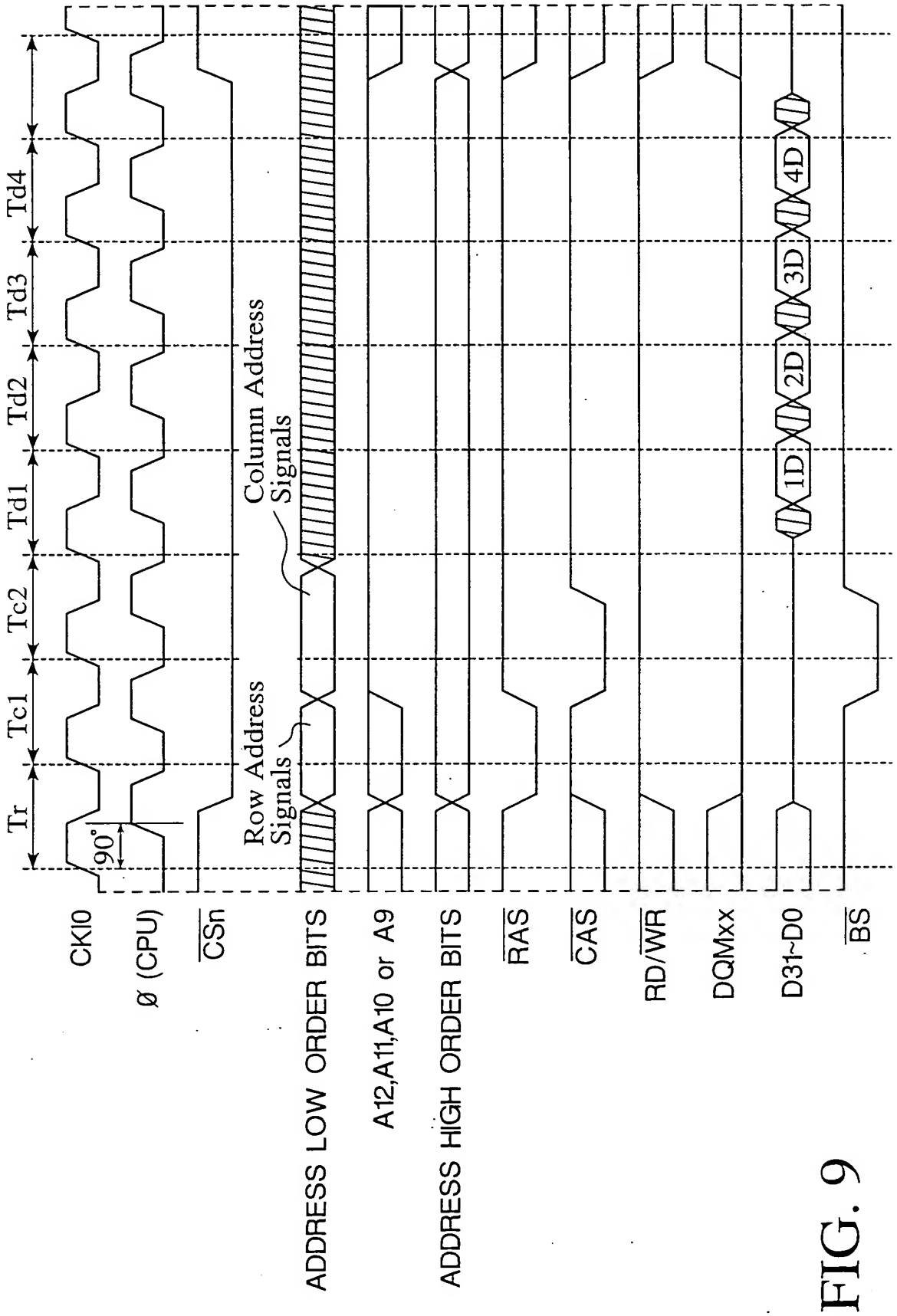

Tr
Tc1
Tc2
Td1
Td2
Td3
Td4
90°
Row Address Signals
Column Address Signals
CKI0
ø (CPU)
CSn
ADDRESS LOW ORDER BITS
A12,A11,A10 or A9
ADDRESS HIGH ORDER BITS
RAS
CAS
RD/WR
DQMxx
D31~D0
BS
1D
2D
3D
4D

FIG. 9

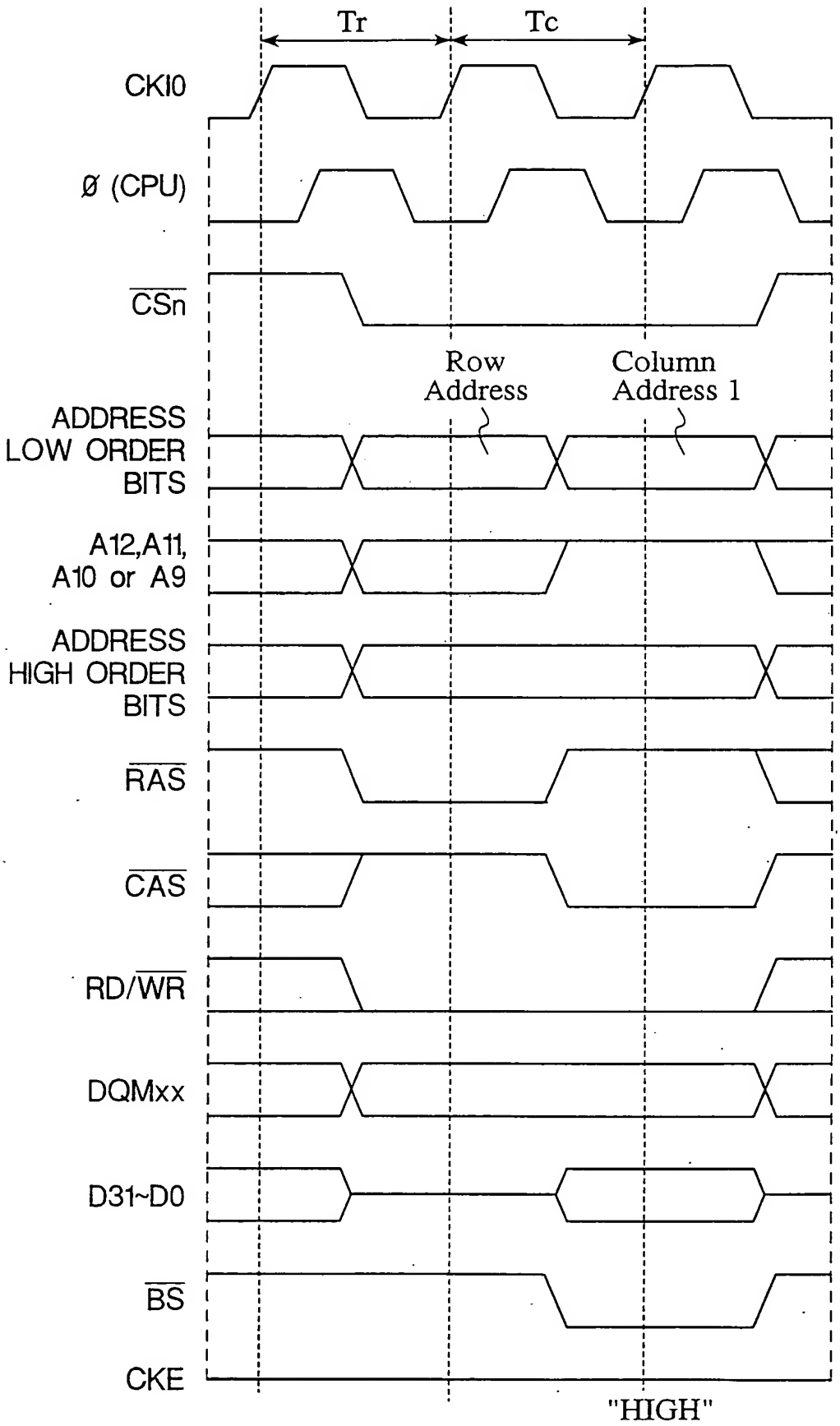

Tr
Tc
CKI0
Ø (CPU)
CSn
Row Address
Column Address 1
ADDRESS LOW ORDER BITS
A12,A11, A10 or A9
ADDRESS HIGH ORDER BITS
RAS
CAS
RD/WR
DQMxx
D31~D0
BS
CKE
"HIGH"

FIG. 10

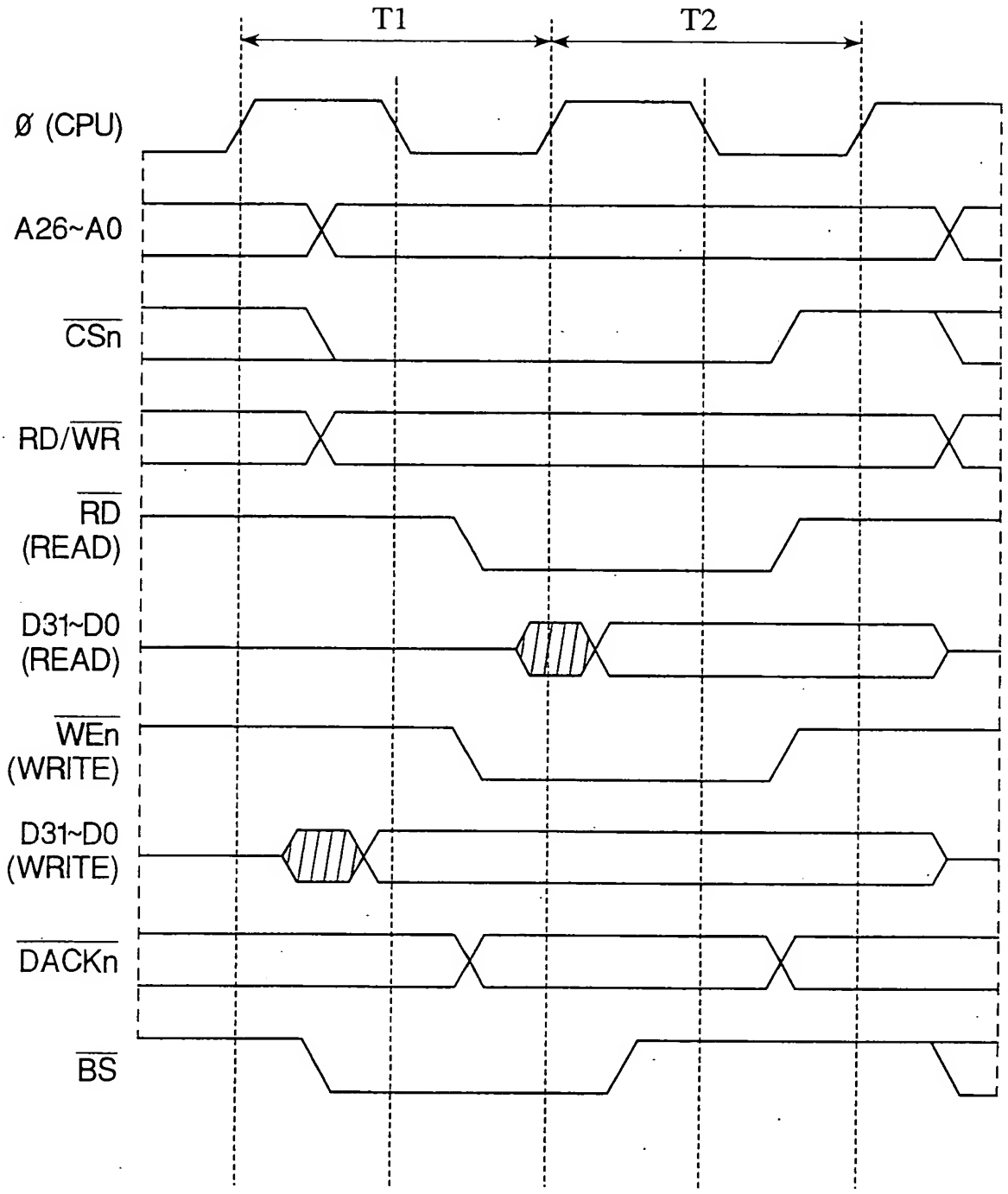

T1
T2
Ø (CPU)
A26~A0
CSn
RD/WR
RD
(READ)
D31~D0
(READ)
WEn
(WRITE)
D31~D0
(WRITE)
DACKn
BS

FIG. 11

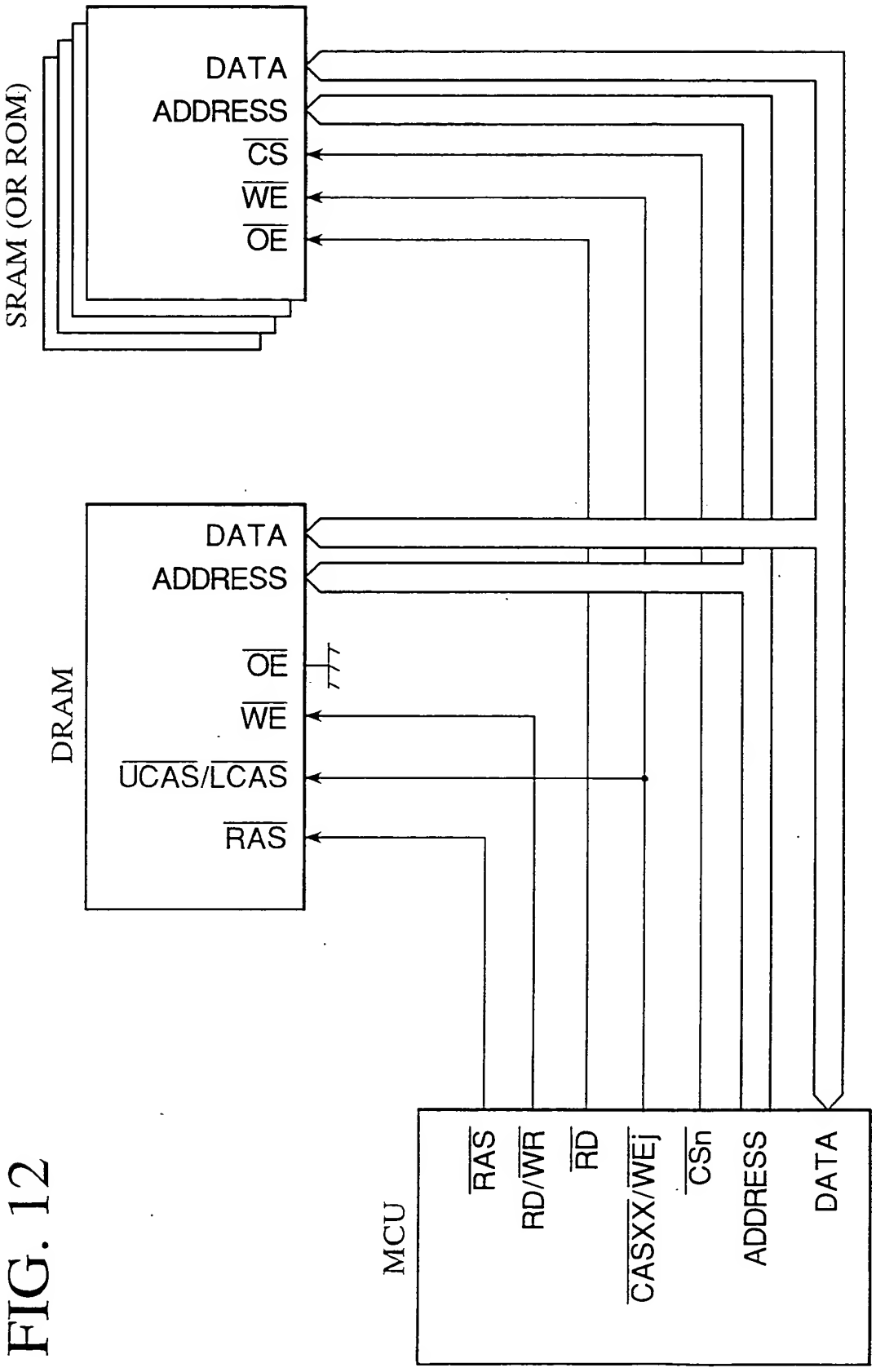

SRAM (OR ROM)
DATA
ADDRESS
CS
WE
OE
DRAM
DATA
ADDRESS
OE
WE
UCAS/LCAS
RAS
MCU
RAS
RD/WR
RD
CASXX/WEj
CSn
ADDRESS
DATA

FIG. 12

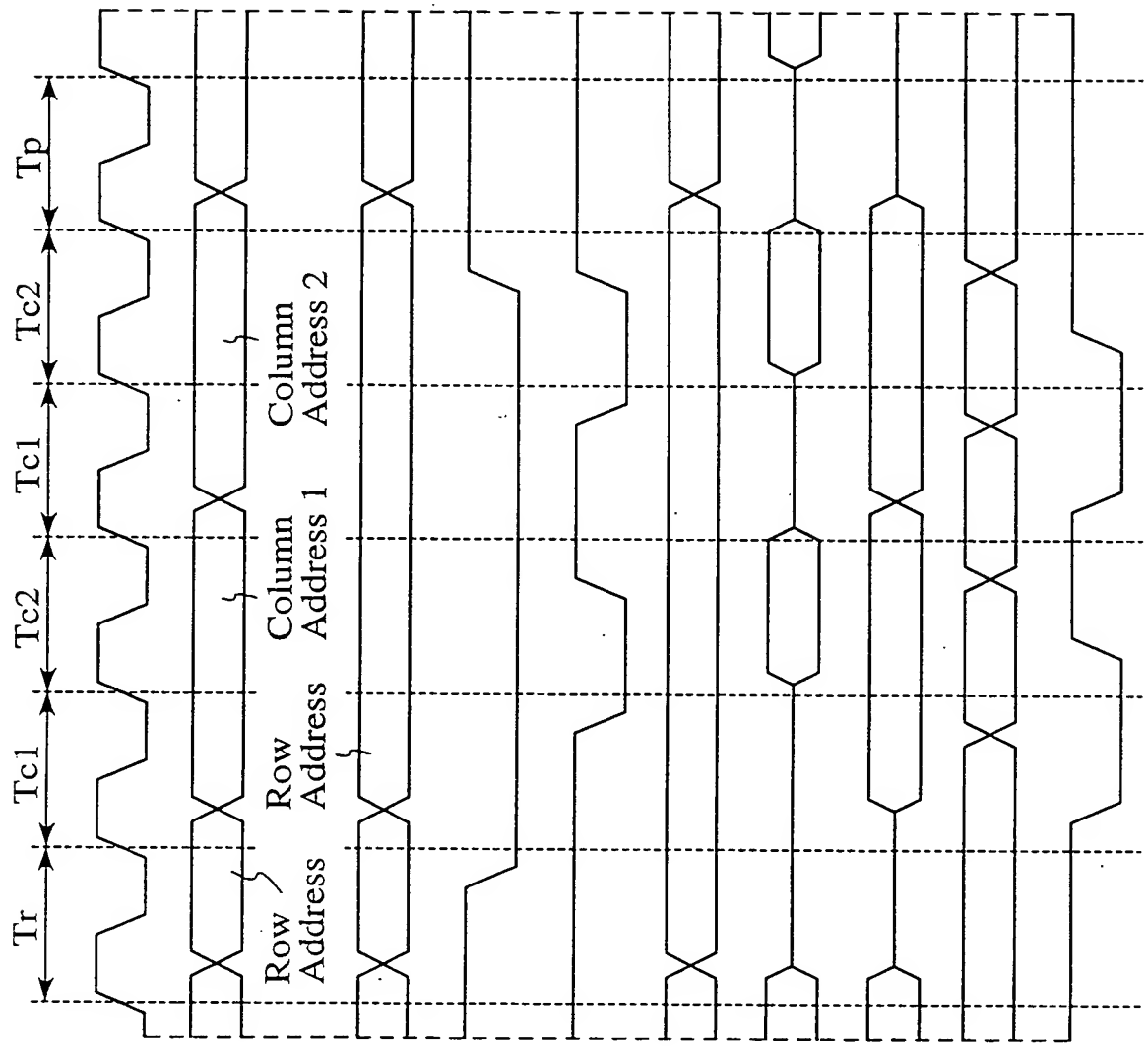

Tr
Tc1
Tc2
Tc1
Tc2
Tp
Ø (CPU)
ADDRESS LOW ORDER BITS
Row Address
Row Address
Column Address 1
Column Address 2
ADDRESS HIGH ORDER BITS
RAS
CASxx
RD/WR
D31~D0 (READ)
D31~D0 (WRITE)
DACKn
BS

FIG. 13

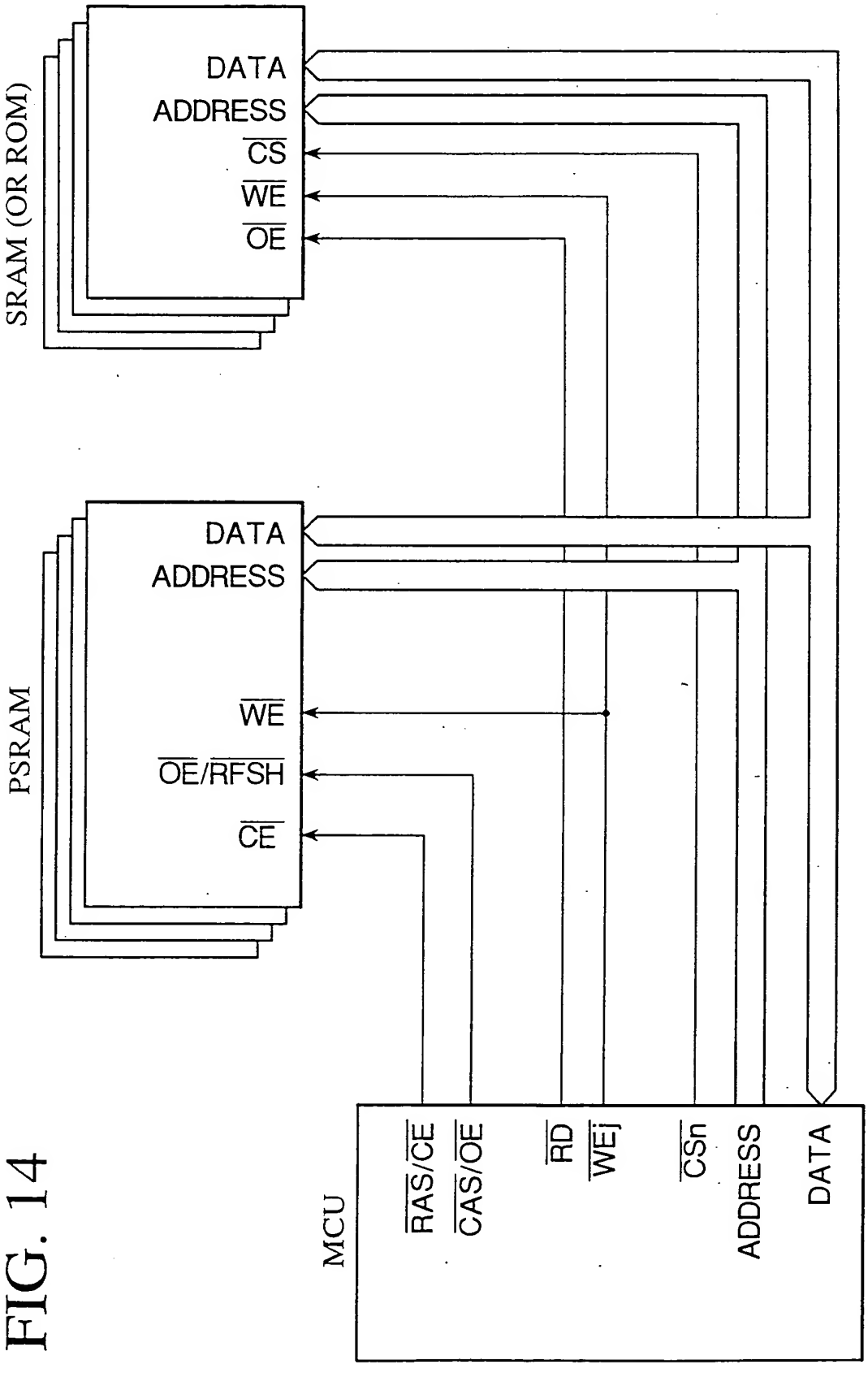

SRAM (OR ROM)
DATA
ADDRESS
CS
WE
OE
PSRAM
DATA
ADDRESS
WE
OE/RFSH
CE
MCU
RAS/CE
CAS/OE
RD
WEj
CSn
ADDRESS
DATA

FIG. 14

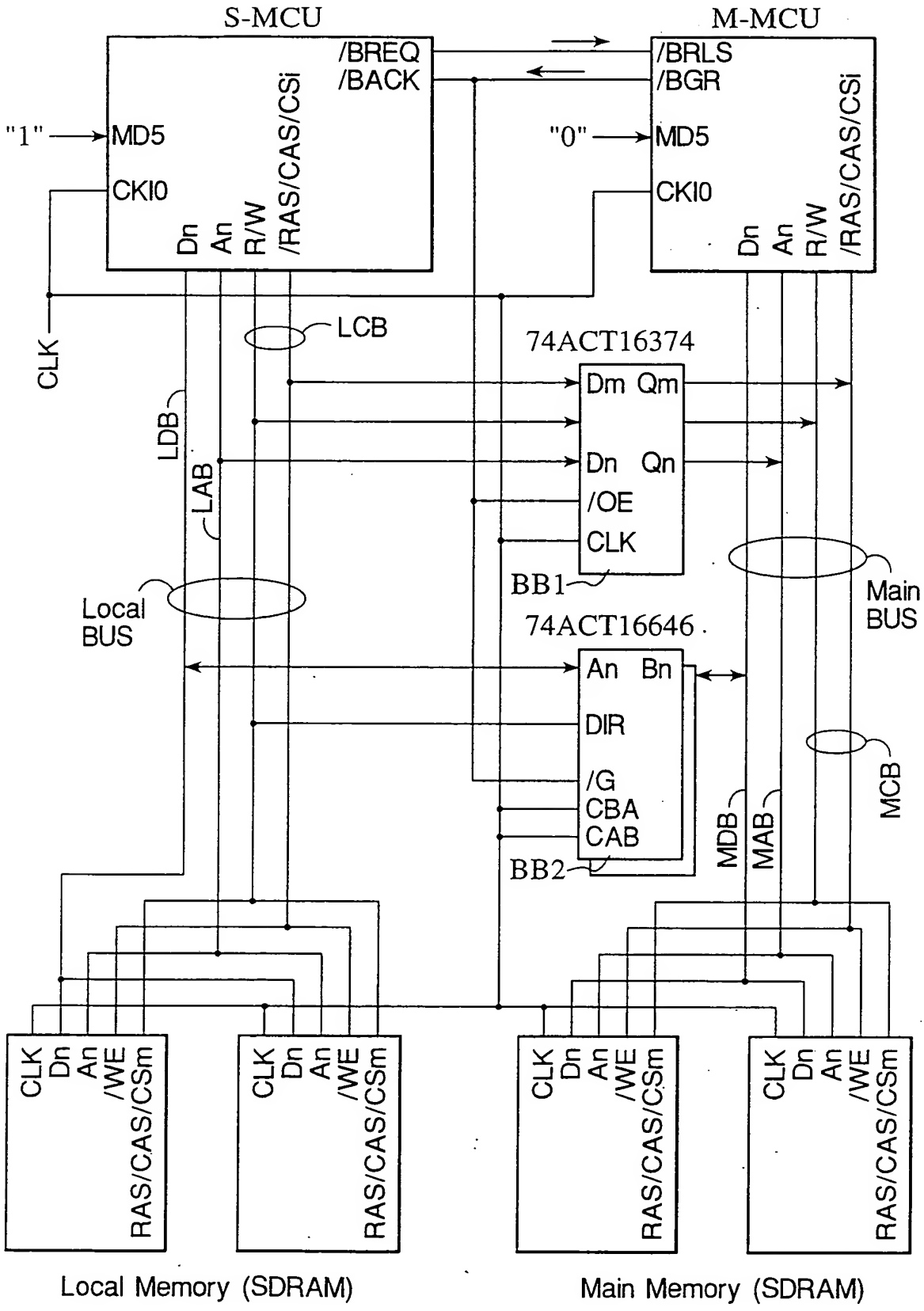

S-MCU
M-MCU
/BREQ
/BACK
/BRLS
/BGR
"1"
MD5
"0"
MD5
CKI0
CKI0
Dn
An
R/W
/RAS/CAS/CSi
CLK
LCB
74ACT16374
Dm Qm
Dn Qn
/OE
CLK
LDB
LAB
BB1
Local
BUS
Main
BUS
74ACT16646
An Bn
DIR
/G
CBA
CAB
BB2
MDB
MAB
MCB
CLK
Dn
An
/WE
RAS/CAS/CSm
Local Memory (SDRAM)
Main Memory (SDRAM)

FIG. 15

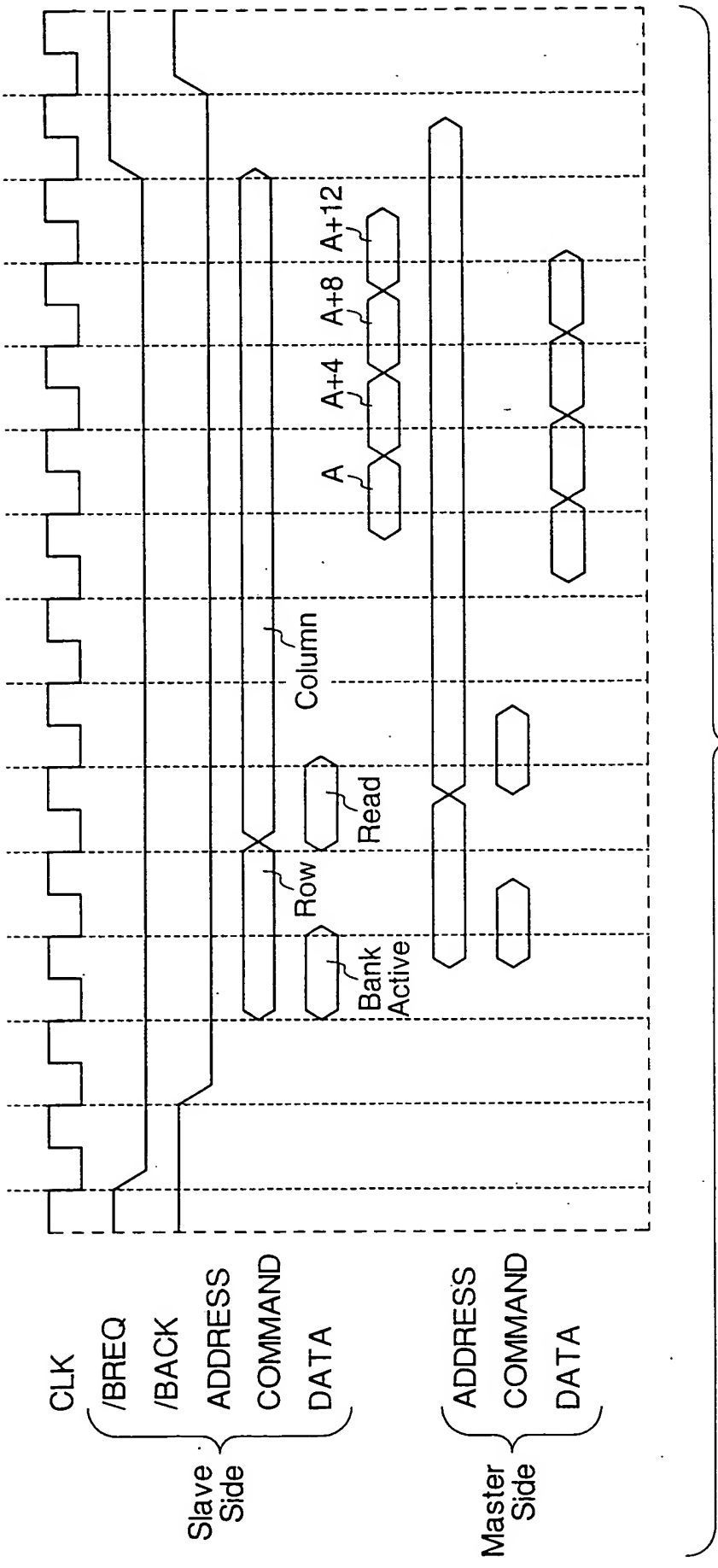

CLK
/BREQ
/BACK
ADDRESS
COMMAND
DATA
Slave Side
ADDRESS
COMMAND
DATA
Master Side
Bank Active
Row
Read
Column
A
A+4
A+8
A+12

FIG. 16

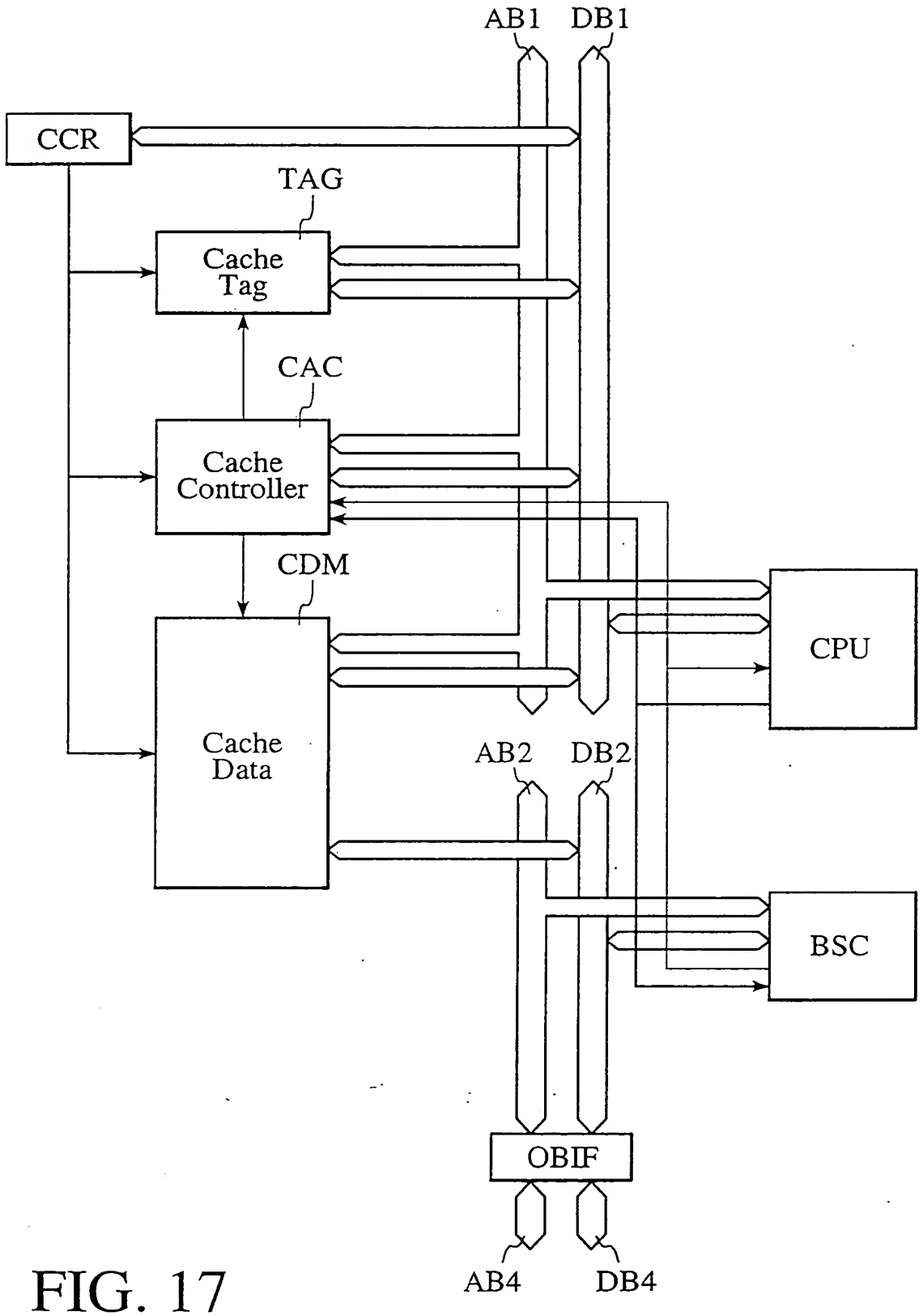

AB1
DB1
CCR
TAG
Cache Tag
CAC
Cache Controller
CDM
Cache Data
CPU
AB2
DB2
BSC
OBIF
AB4
DB4

FIG. 17

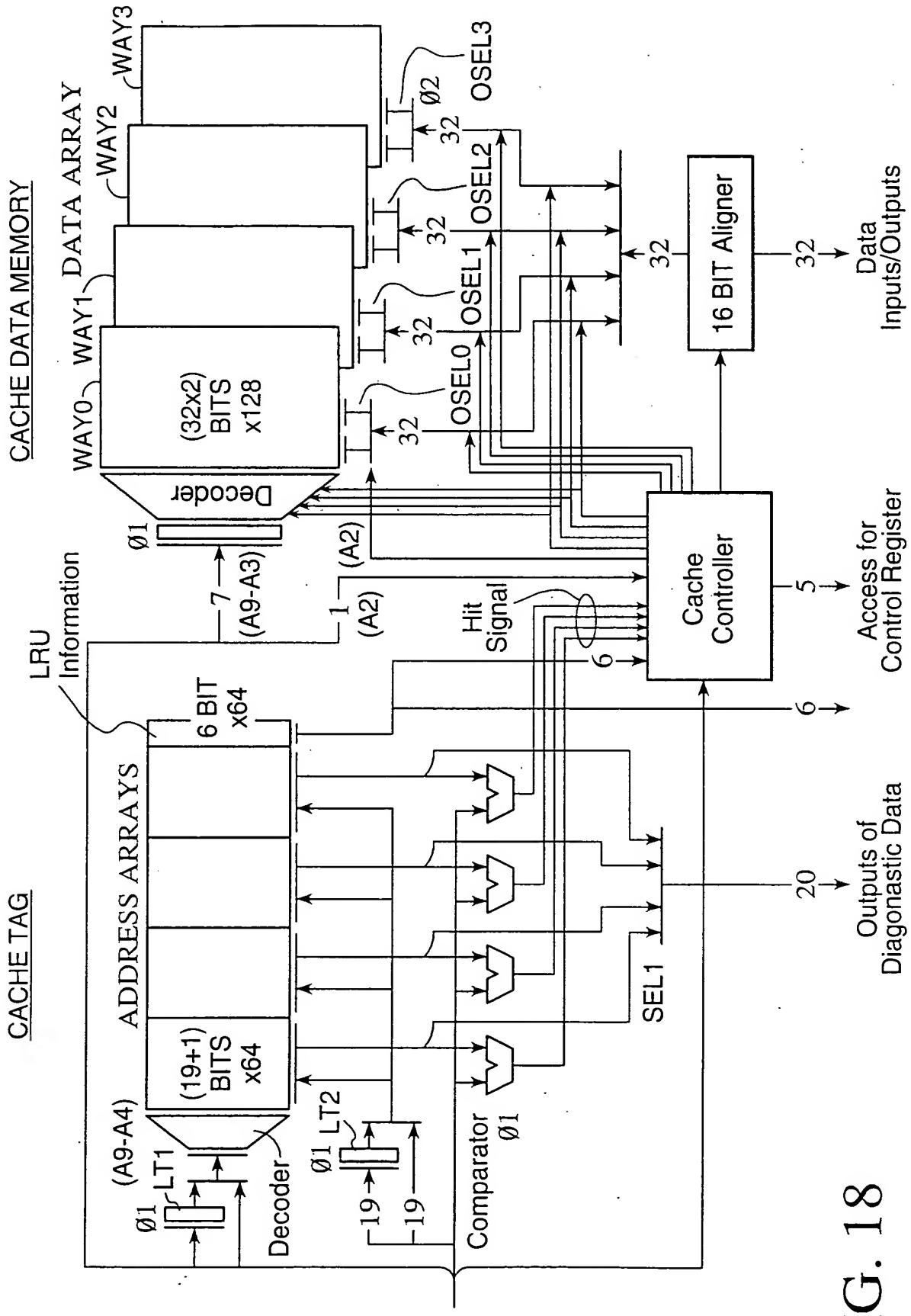

CACHE DATA MEMORY
DATA ARRAY
WAY0
WAY1
WAY2
WAY3
(32x2) BITS x128
Decoder
Ø1
7 (A9-A3)
1 (A2)
(A2)
32
OSEL0
OSEL1
OSEL2
OSEL3
Ø2
16 BIT Aligner
Data Inputs/Outputs
Hit Signal
Cache Controller
5
Access for Control Register
6
LRU Information
6 BIT x64
CACHE TAG
ADDRESS ARRAYS
(19+1) BITS x64
(A9-A4)
LT1
LT2
Decoder
19
Comparator
SEL1
20
Outputs of Diagonastic Data

FIG. 18

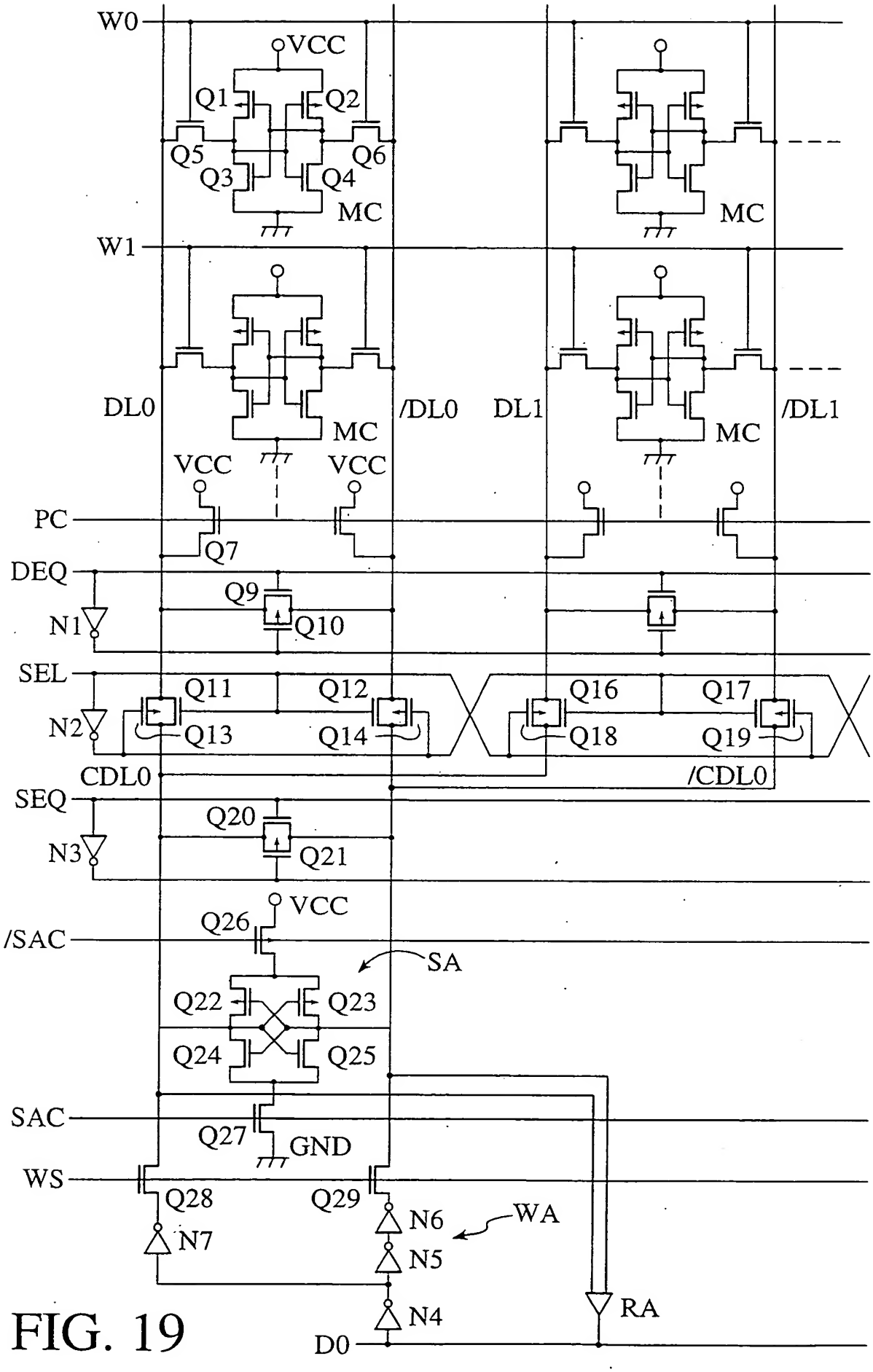

W0
VCC
Q1
Q2
Q5
Q6
Q3
Q4
MC
W1
DL0
/DL0
DL1
/DL1
VCC
VCC
PC
Q7
DEQ
Q9
N1
Q10
SEL
Q11
Q12
Q16
Q17
N2
Q13
Q14
Q18
Q19
CDL0
/CDL0
SEQ
Q20
N3
Q21
VCC
Q26
/SAC
SA
Q22
Q23
Q24
Q25
SAC
Q27
GND
WS
Q28
Q29
N6
WA
N7
N5
N4
RA
D0

FIG. 19

FIG. 20

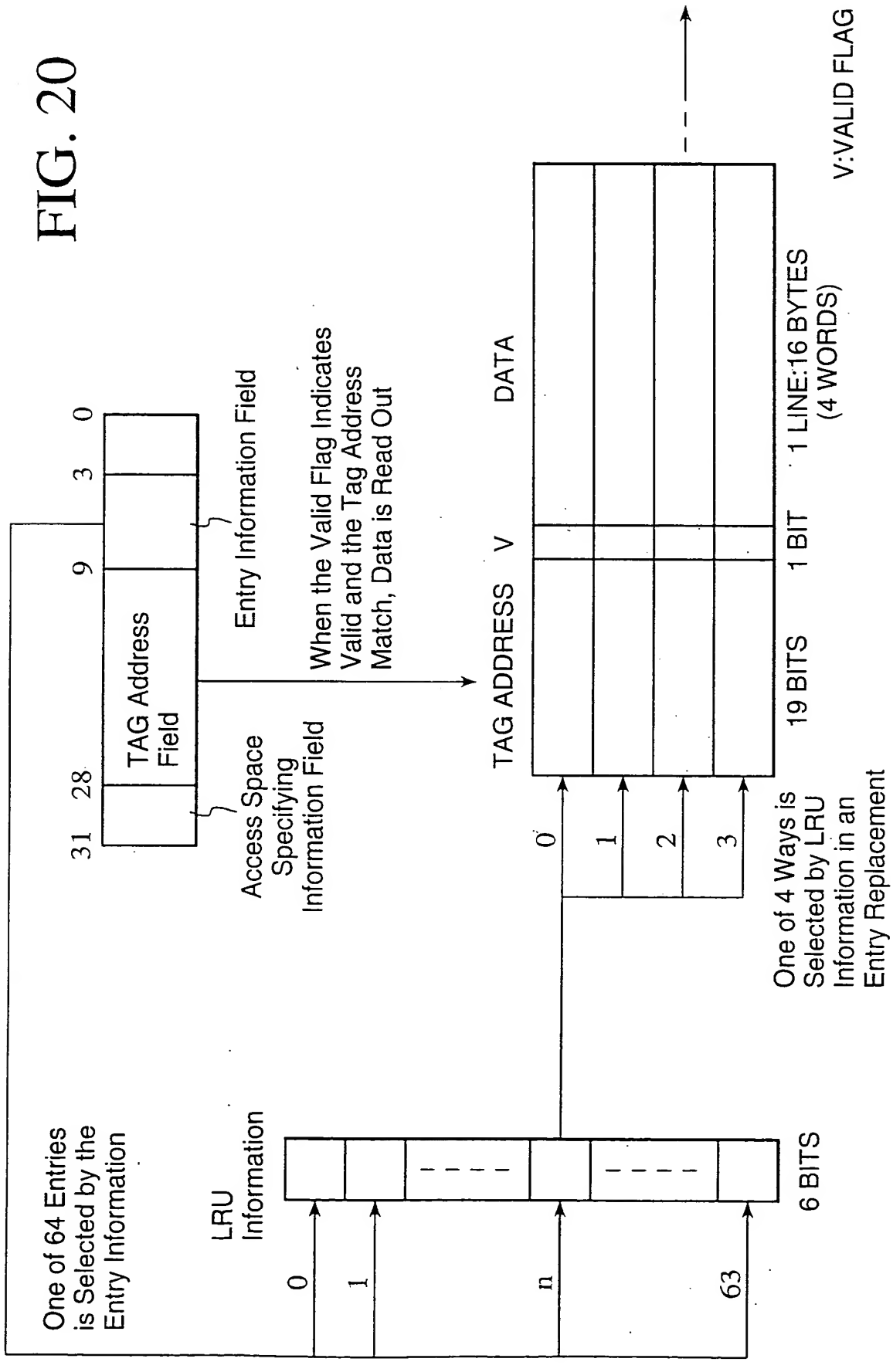
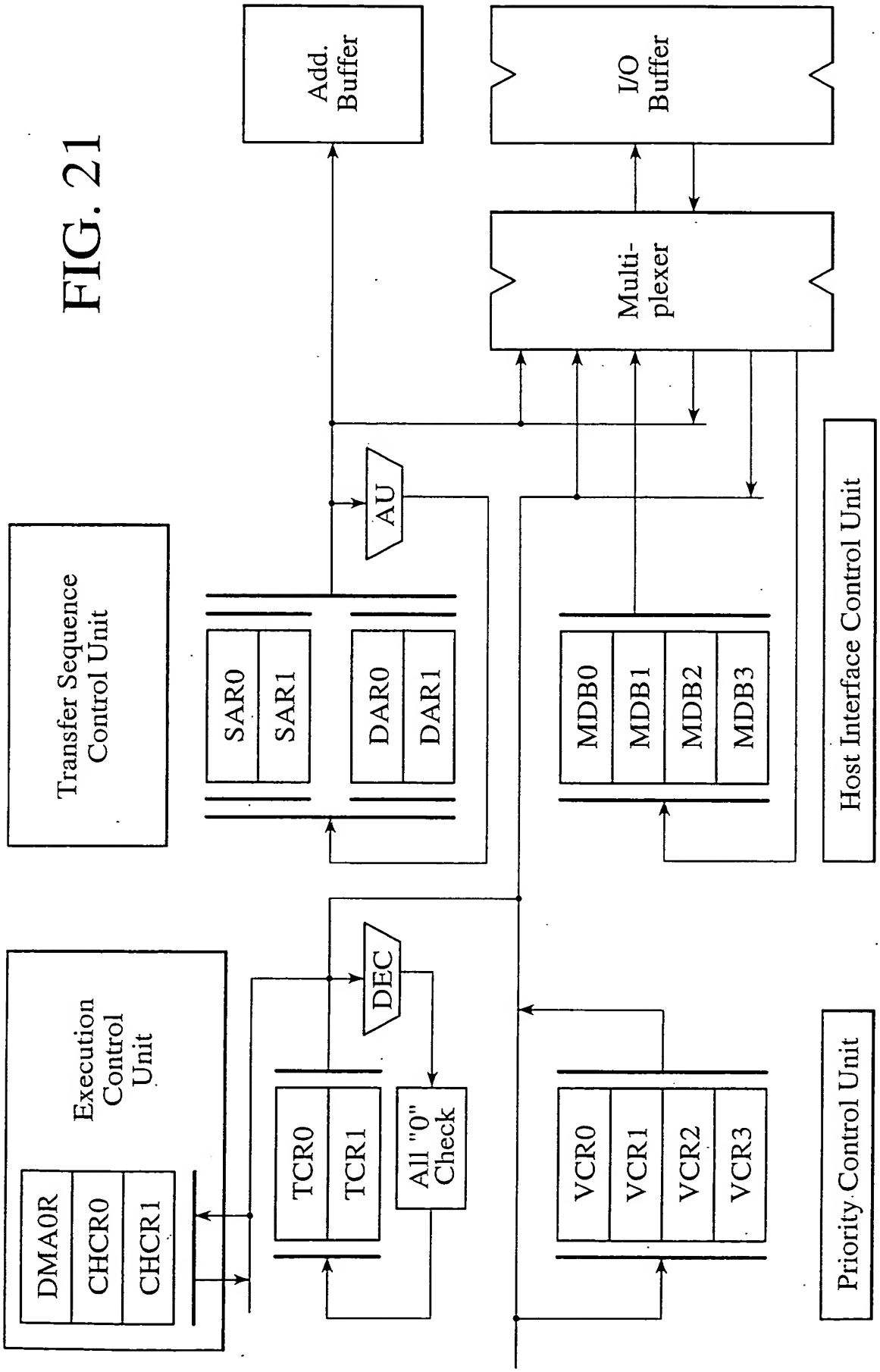

One of 64 Entries is Selected by the Entry Information
LRU Information
0
1
n
63
6 BITS
31 28
TAG Address Field
9
3 0
Entry Information Field
Access Space Specifying Information Field
When the Valid Flag Indicates Valid and the Tag Address Match, Data is Read Out
TAG ADDRESS
V
DATA
19 BITS
1 BIT
1 LINE:16 BYTES (4 WORDS)
0
1
2
3
One of 4 Ways is Selected by LRU Information in an Entry Replacement
V:VALID FLAG

FIG. 21


Add. Buffer
I/O Buffer
Multi-plexer
Transfer Sequence Control Unit
AU
SAR0
SAR1
DAR0
DAR1
MDB0
MDB1
MDB2
MDB3
Host Interface Control Unit
Execution Control Unit
DMA0R
CHCR0
CHCR1
DEC
TCR0
TCR1
All "0" Check
VCR0
VCR1
VCR2
VCR3
Priority Control Unit

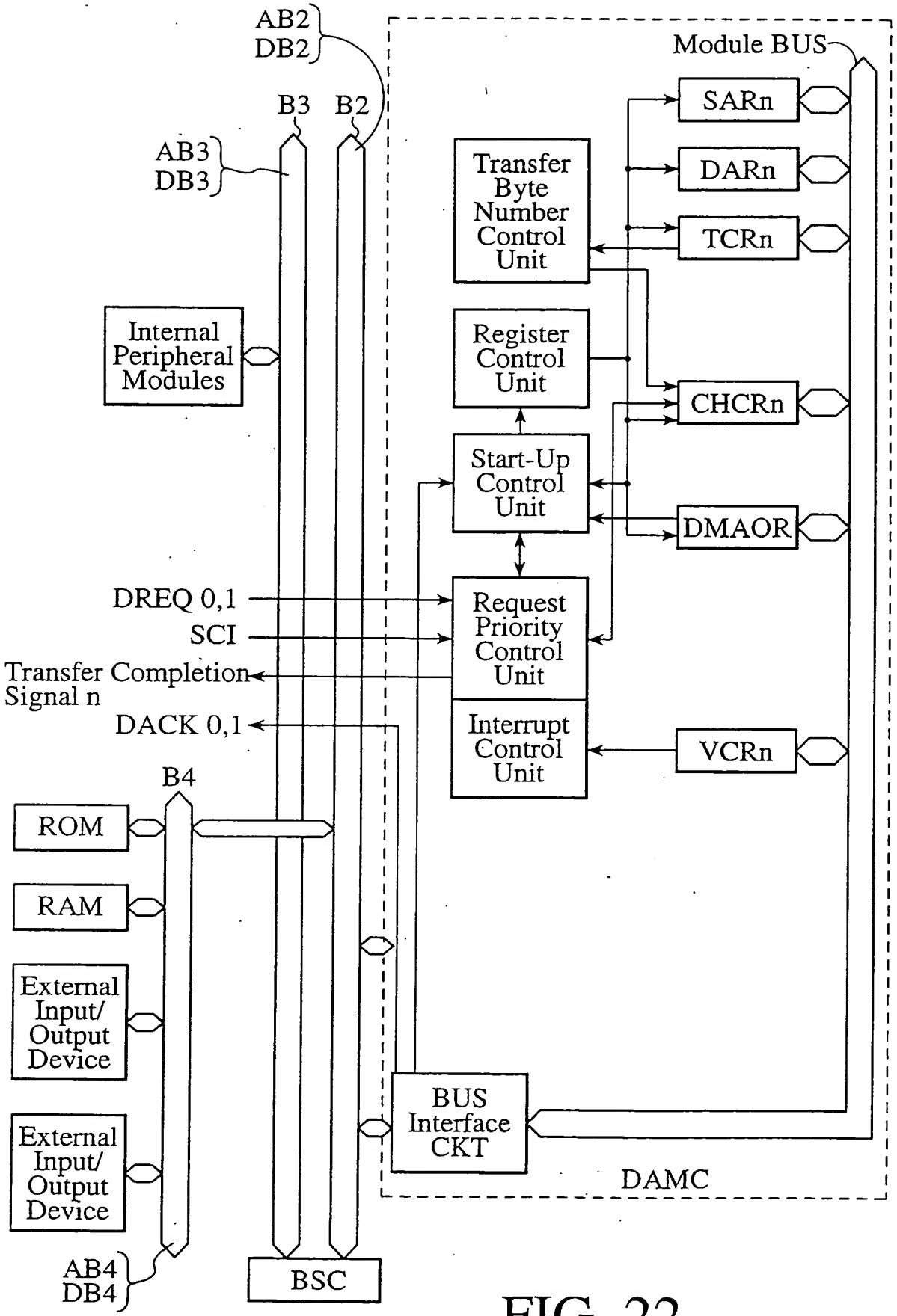

AB2
DB2
B3
B2
AB3
DB3
Module BUS
SARn
DARn
TCRn
Transfer Byte Number Control Unit
Internal Peripheral Modules
Register Control Unit
CHCRn
Start-Up Control Unit
DMAOR
DREQ 0,1
SCI
Transfer Completion Signal n
DACK 0,1
Request Priority Control Unit
Interrupt Control Unit
VCRn
B4
ROM
RAM
External Input/ Output Device
External Input/ Output Device
BUS Interface CKT
DAMC
AB4
DB4
BSC

FIG. 22

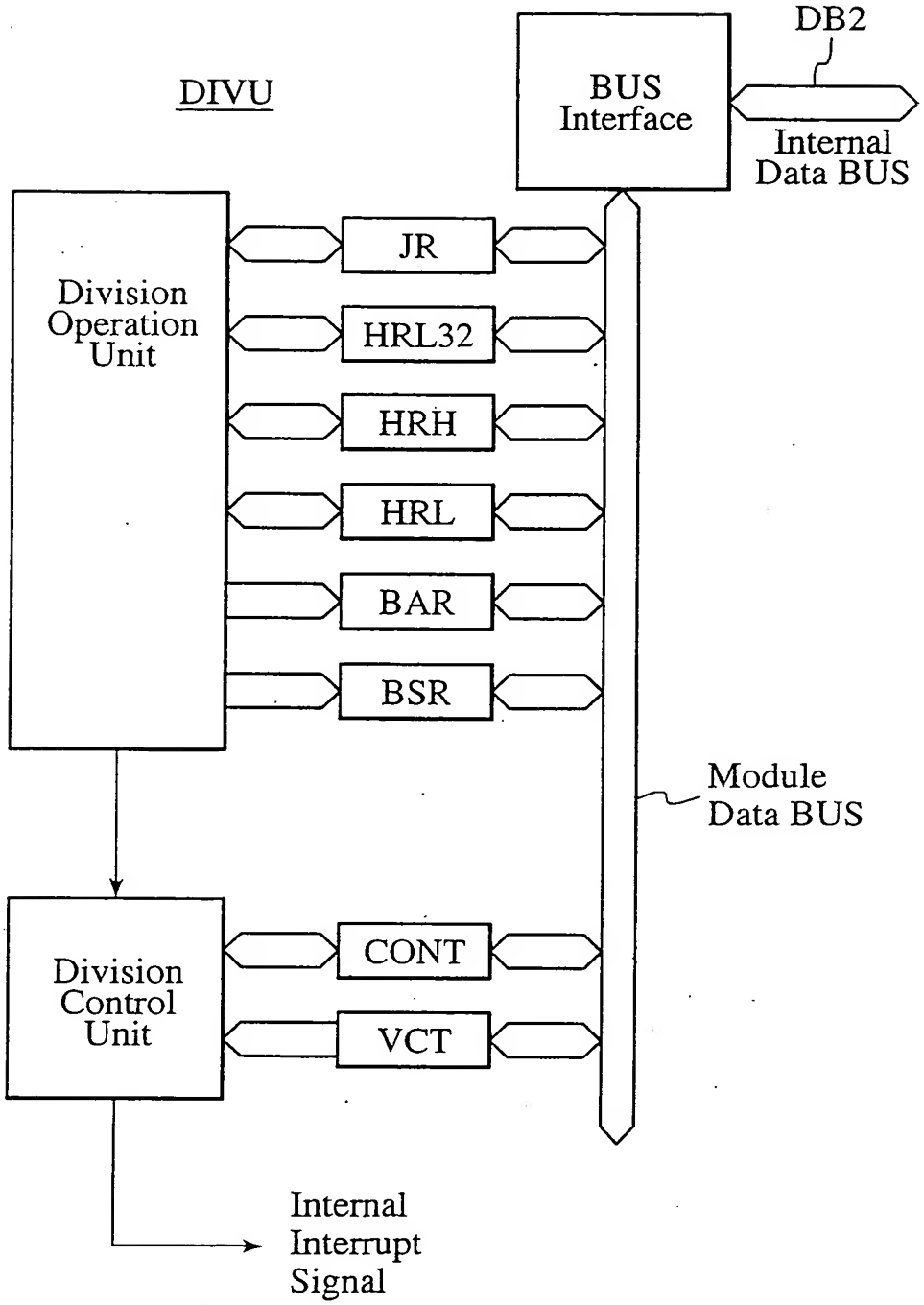

DIVU
BUS Interface
DB2
Internal Data BUS
Division Operation Unit
JR
HRL32
HRH
HRL
BAR
BSR
Module Data BUS
Division Control Unit
CONT
VCT
Internal Interrupt Signal

FIG. 23

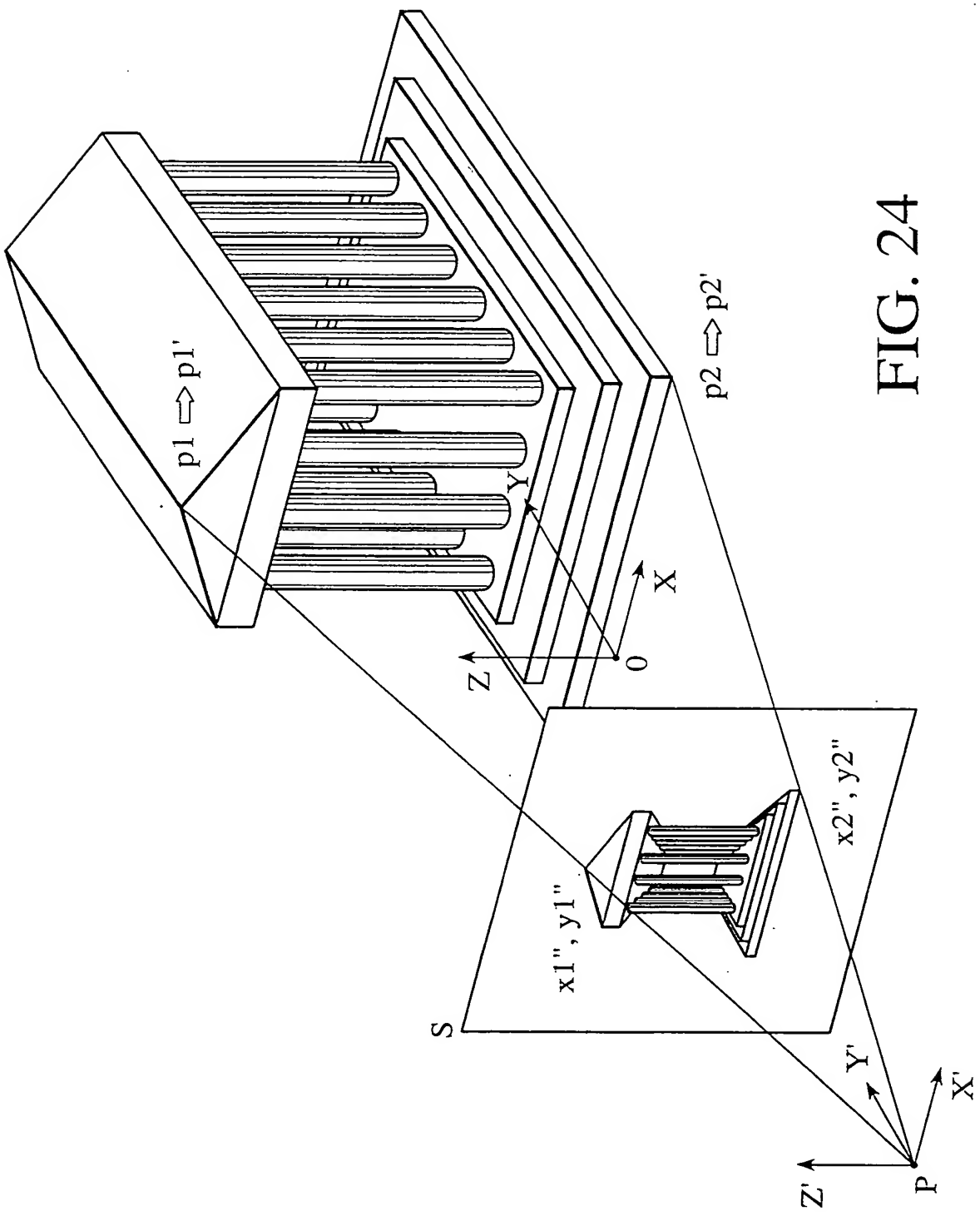


FIG. 24

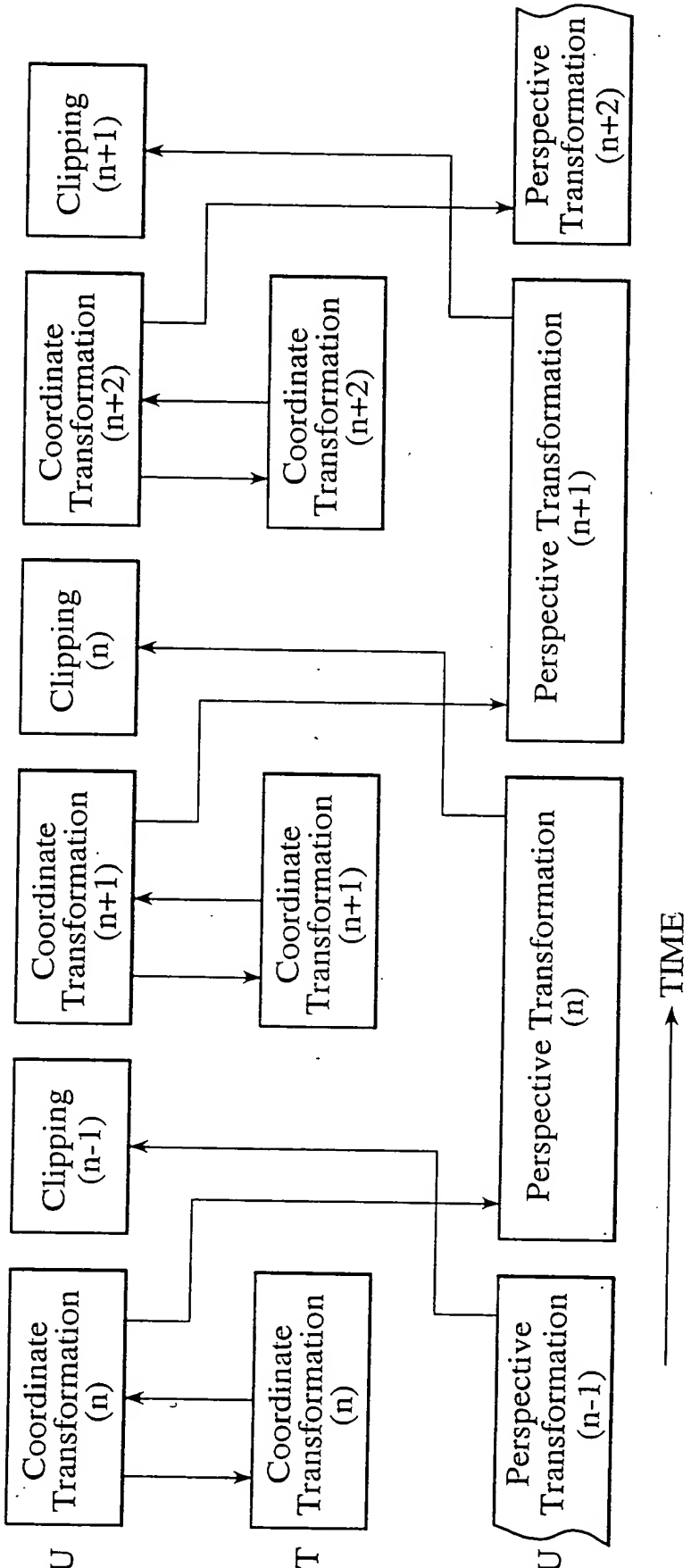

CPU
MULT
DIVU
TIME
Coordinate Transformation (n)
Coordinate Transformation (n)
Clipping (n-1)
Perspective Transformation (n-1)
Coordinate Transformation (n+1)
Coordinate Transformation (n+1)
Clipping (n)
Perspective Transformation (n)
Coordinate Transformation (n+2)
Coordinate Transformation (n+2)
Clipping (n+1)
Perspective Transformation (n+1)
Perspective Transformation (n+2)

FIG. 25

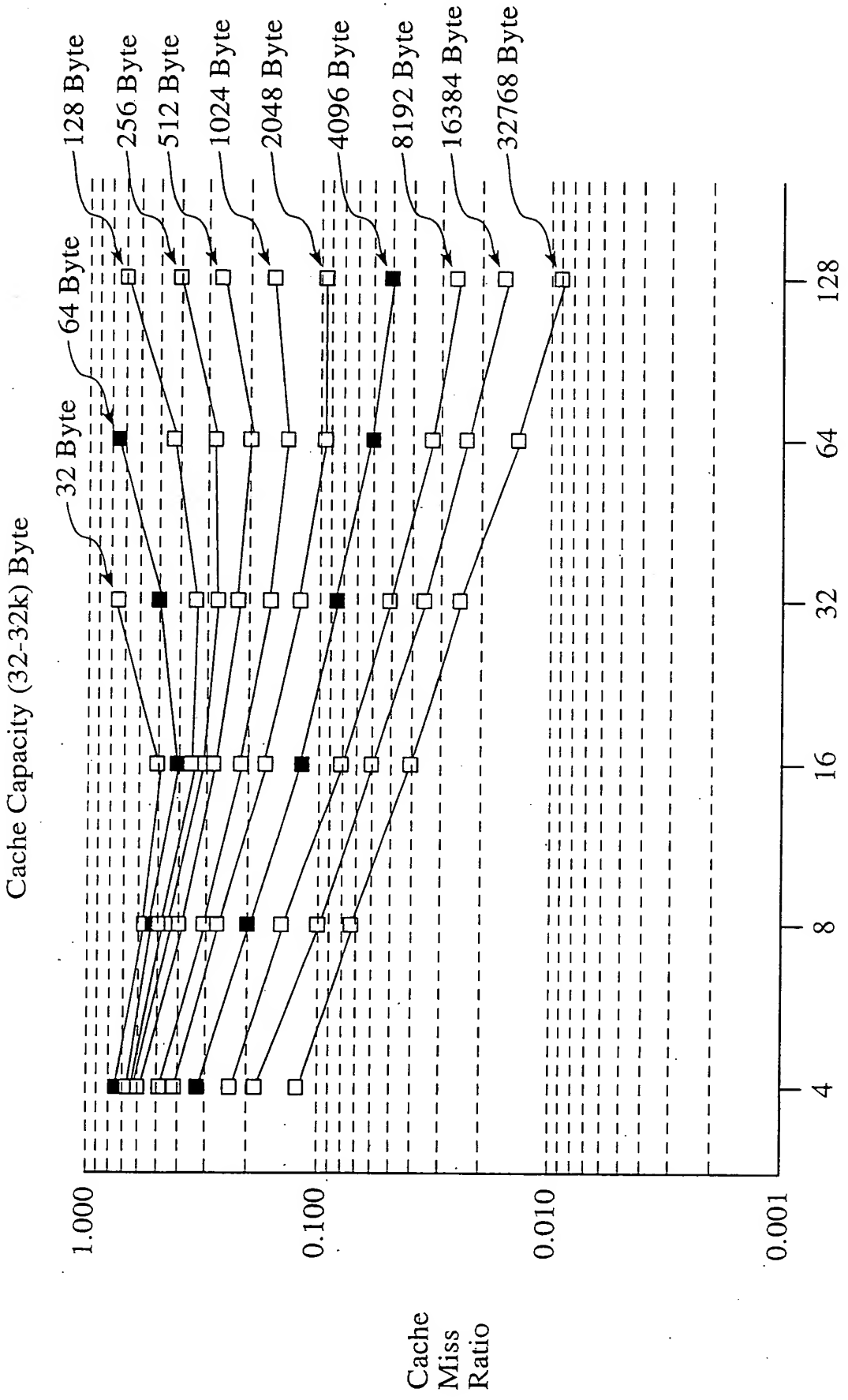

Cache Capacity (32-32k) Byte
32 Byte
64 Byte
128 Byte
256 Byte
512 Byte
1024 Byte
2048 Byte
4096 Byte
8192 Byte
16384 Byte
32768 Byte
Cache Miss Ratio
1.000
0.100
0.010
0.001
4
8
16
32
64
128
Line Size (Byte)

FIG. 26

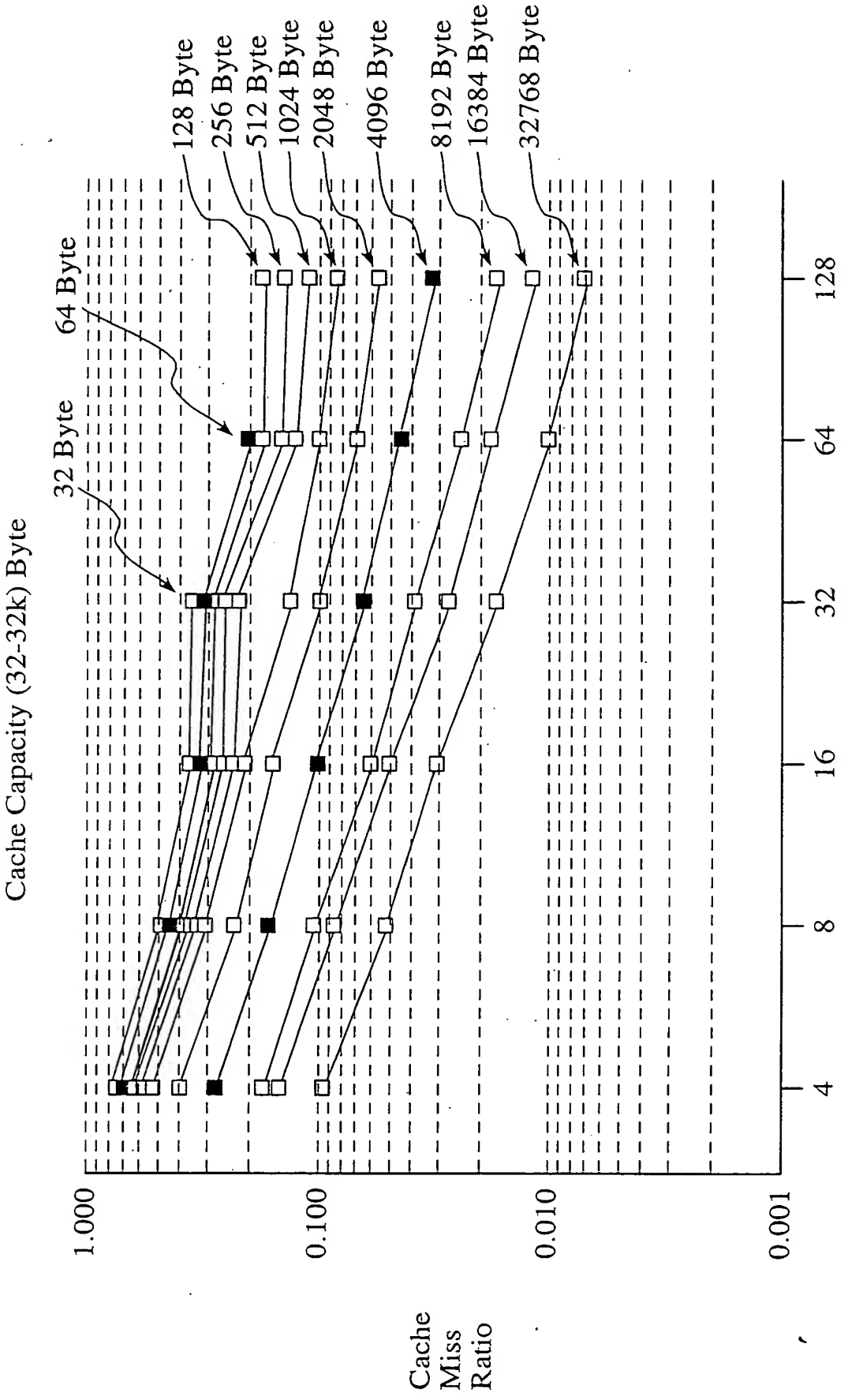

Cache Capacity (32-32k) Byte
32 Byte
64 Byte
128 Byte
256 Byte
512 Byte
1024 Byte
2048 Byte
4096 Byte
8192 Byte
16384 Byte
32768 Byte
1.000
0.100
0.010
0.001
Cache Miss Ratio
4
8
16
32
64
128
Line Size (Byte)

FIG. 27

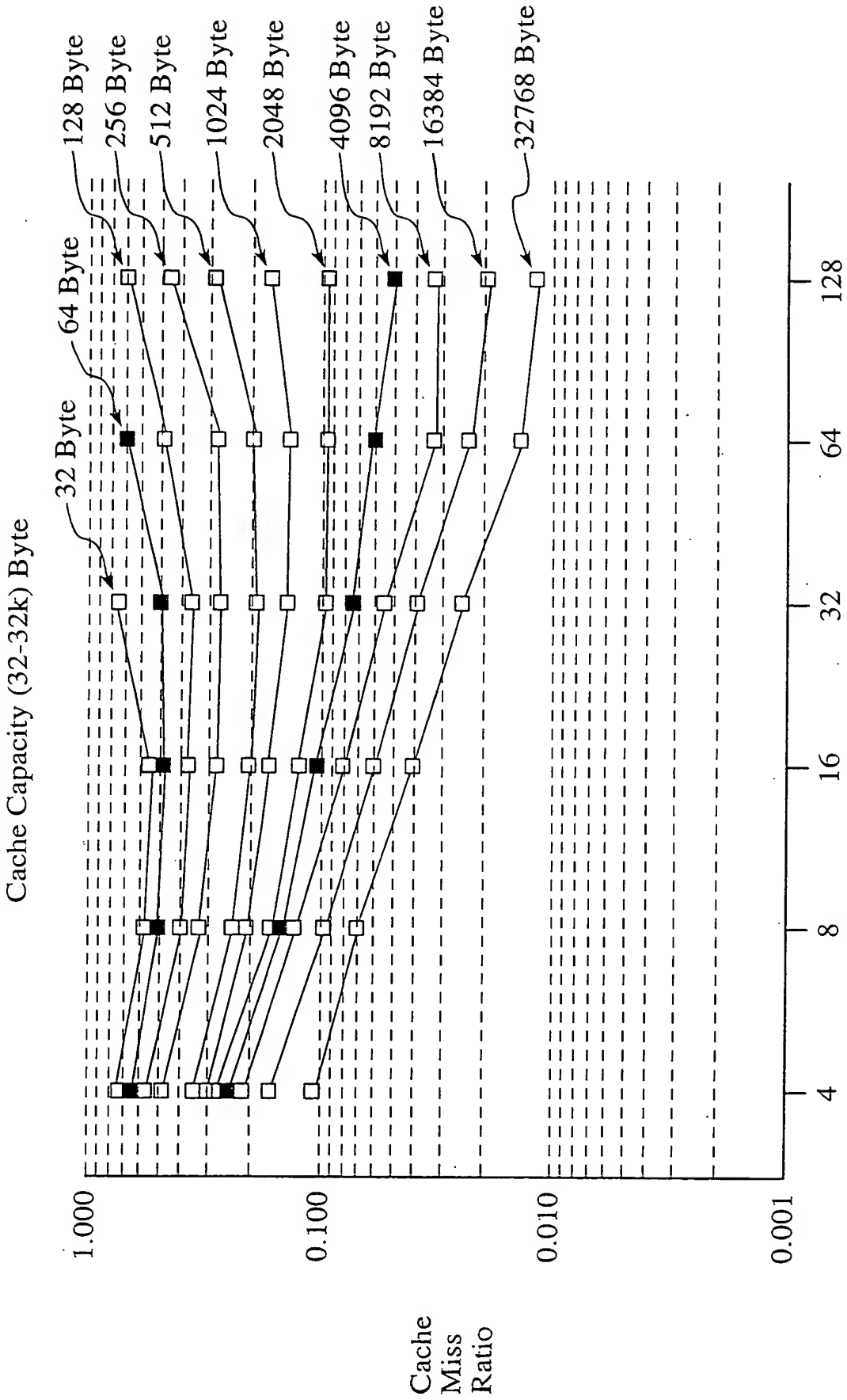

Cache Capacity (32-32k) Byte
32 Byte
64 Byte
128 Byte
256 Byte
512 Byte
1024 Byte
2048 Byte
4096 Byte
8192 Byte
16384 Byte
32768 Byte
Cache Miss Ratio
1.000
0.100
0.010
0.001
4
8
16
32
64
128
Line Size (Byte)

FIG. 28

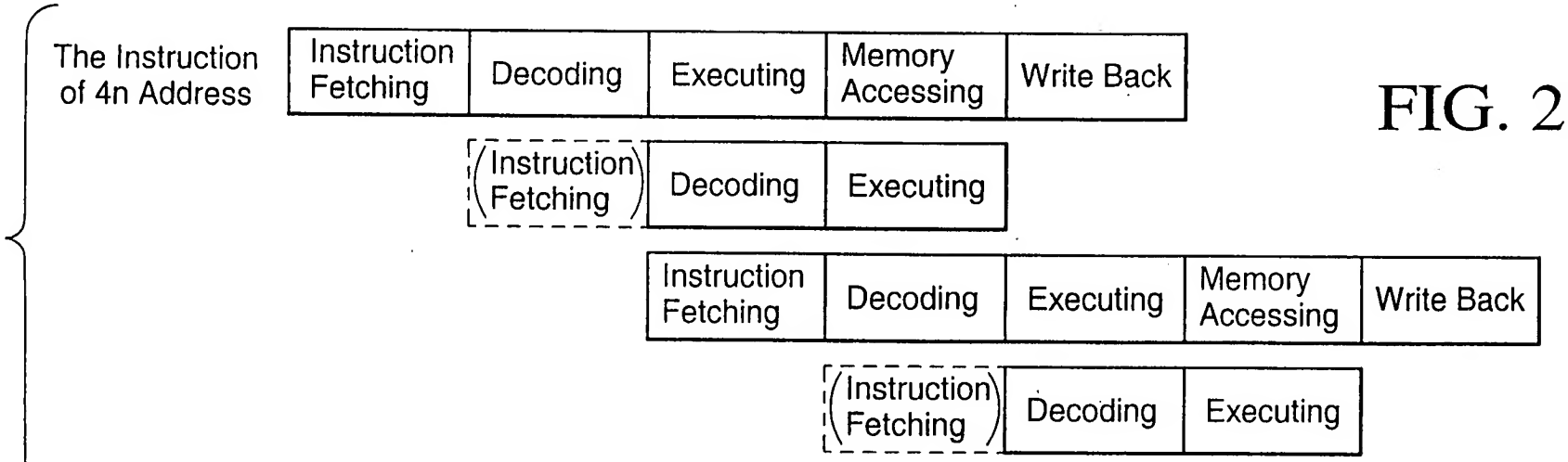


FIG. 29A

In Case of a Memory Access to 4n Address

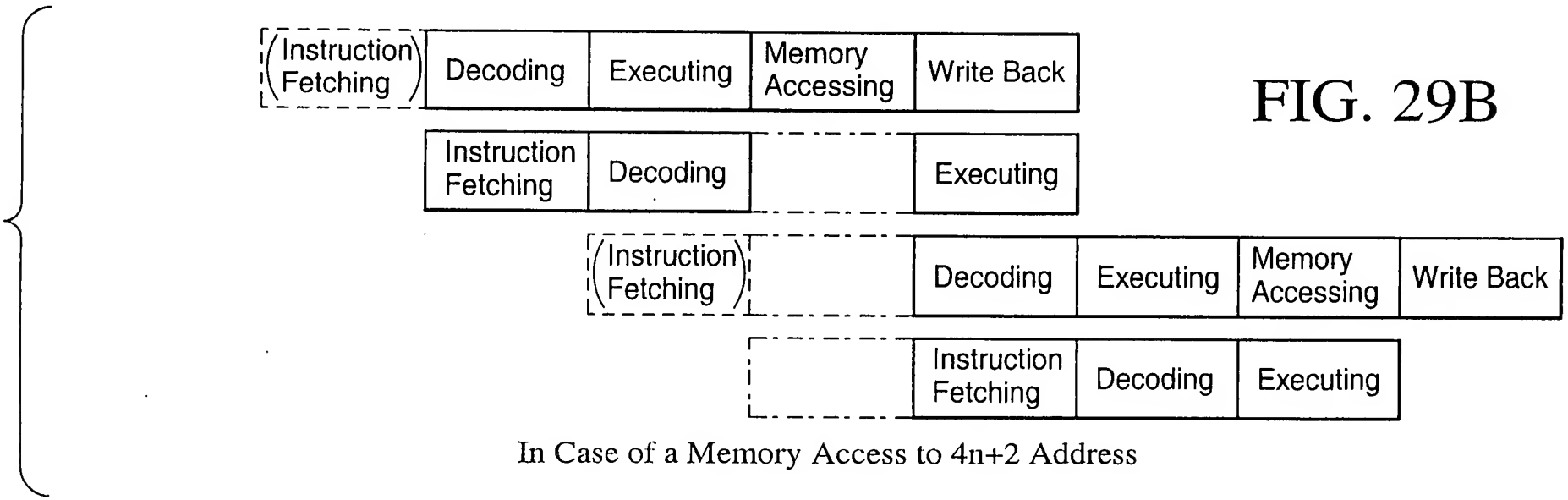


FIG. 29B

In Case of a Memory Access to 4n+2 Address

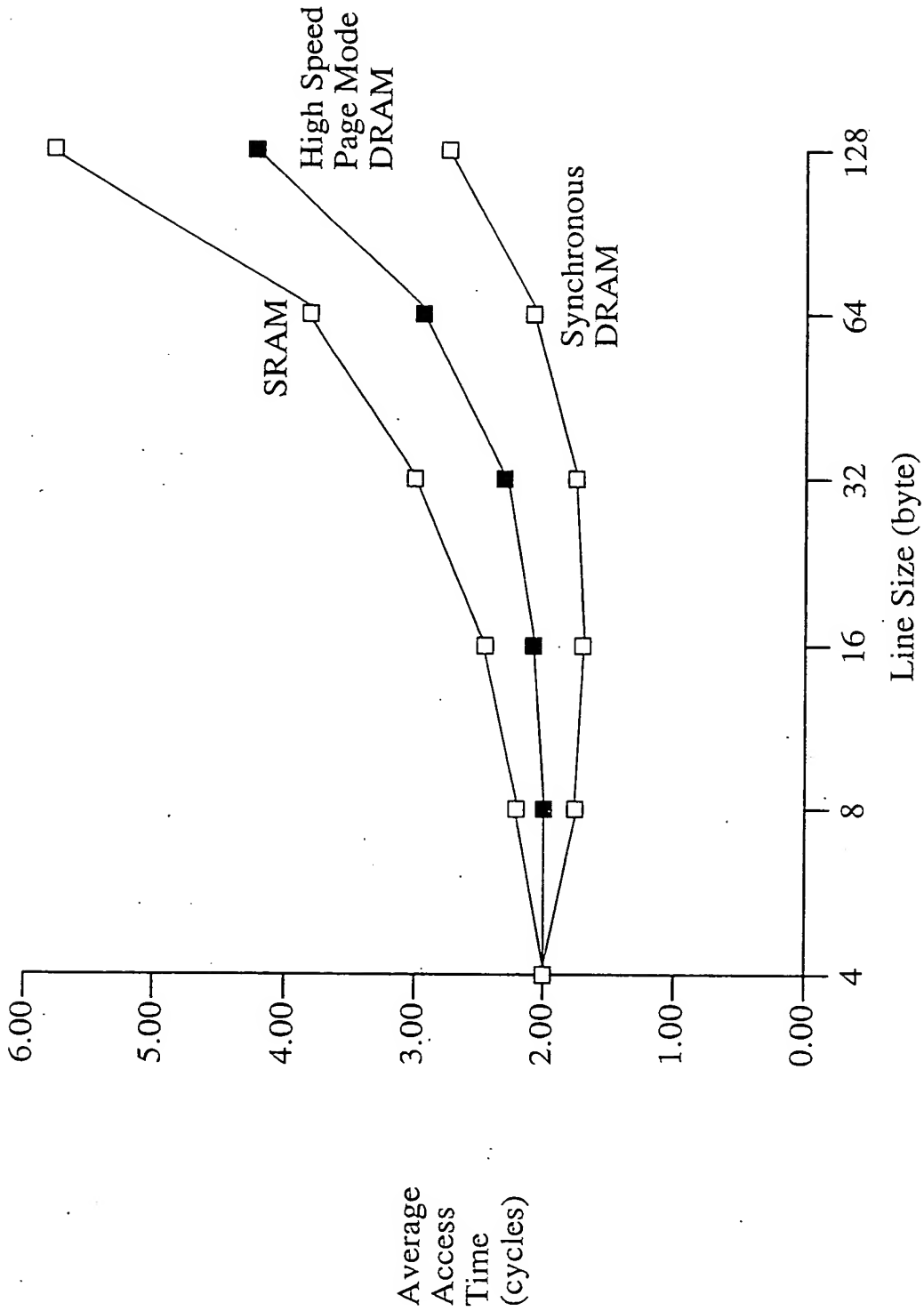

6.00
5.00
4.00
3.00
2.00
1.00
0.00
Average Access Time (cycles)
4
8
16
32
64
128
Line Size (byte)
SRAM
High Speed Page Mode DRAM
Synchronous DRAM

FIG. 30

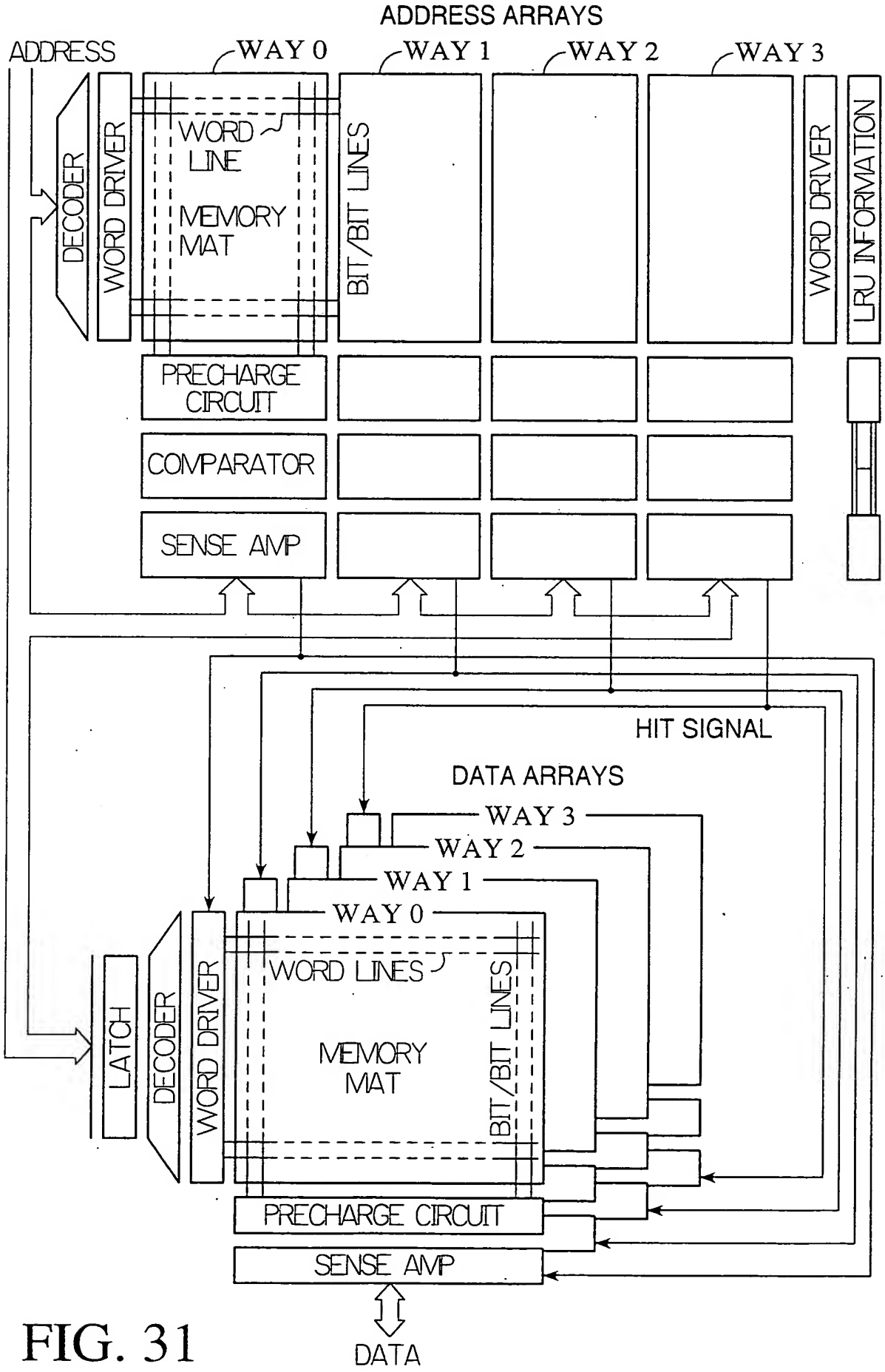

ADDRESS ARRAYS
ADDRESS
WAY 0
WAY 1
WAY 2
WAY 3
DECODER
WORD DRIVER
WORD LINE
MEMORY MAT
BIT/BIT LINES
WORD DRIVER
LRU INFORMATION
PRECHARGE CIRCUIT
COMPARATOR
SENSE AMP
HIT SIGNAL
DATA ARRAYS
WAY 3
WAY 2
WAY 1
WAY 0
LATCH
DECODER
WORD DRIVER
WORD LINES
MEMORY MAT
BIT/BIT LINES
PRECHARGE CIRCUIT
SENSE AMP
DATA

FIG. 31

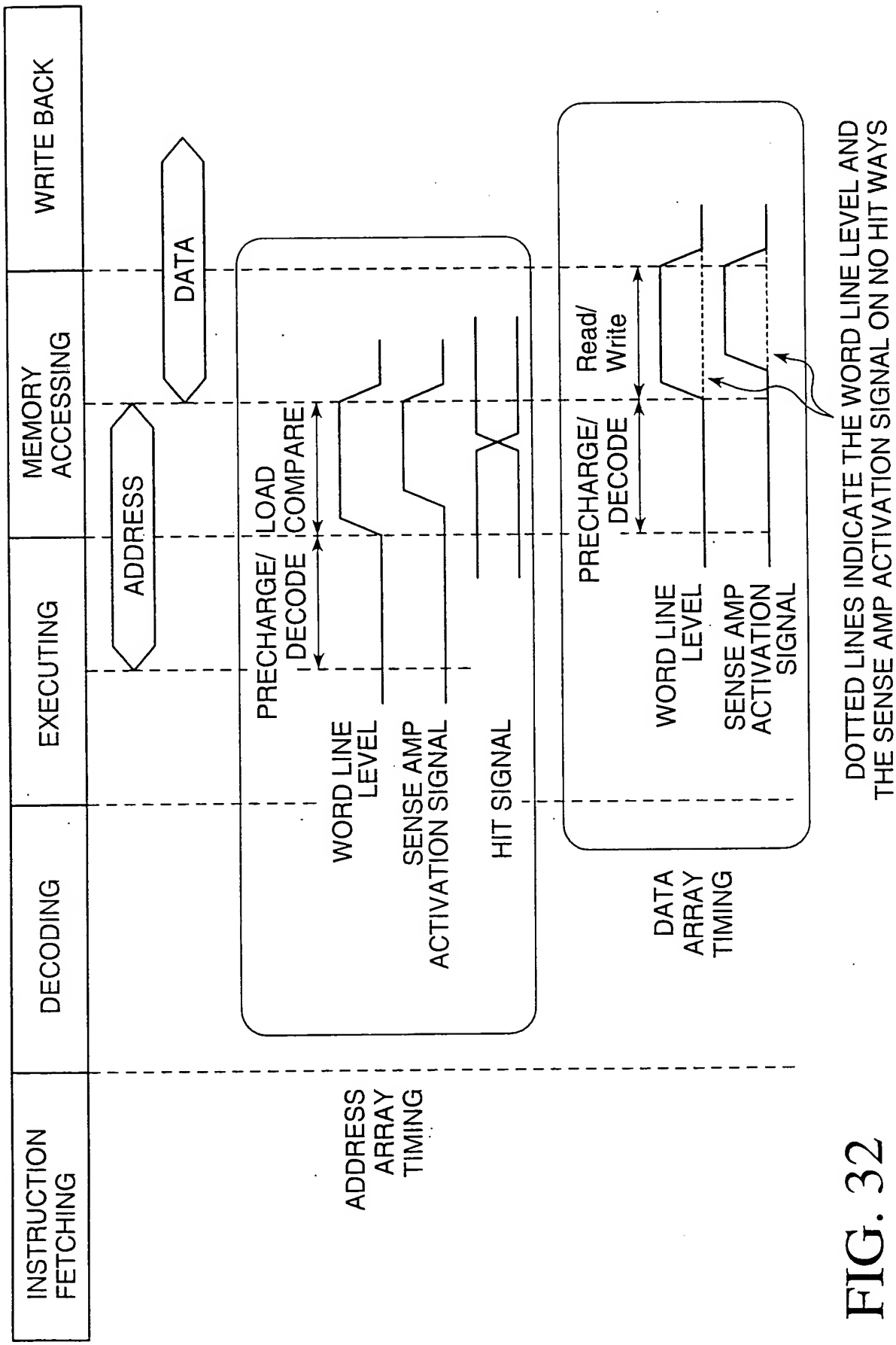

INSTRUCTION FETCHING
DECODING
EXECUTING
MEMORY ACCESSING
WRITE BACK
ADDRESS
DATA
PRECHARGE/ DECODE
LOAD COMPARE
WORD LINE LEVEL
SENSE AMP ACTIVATION SIGNAL
HIT SIGNAL
ADDRESS ARRAY TIMING
PRECHARGE/ DECODE
Read/ Write
WORD LINE LEVEL
SENSE AMP ACTIVATION SIGNAL
DATA ARRAY TIMING
DOTTED LINES INDICATE THE WORD LINE LEVEL AND THE SENSE AMP ACTIVATION SIGNAL ON NO HIT WAYS

FIG. 32

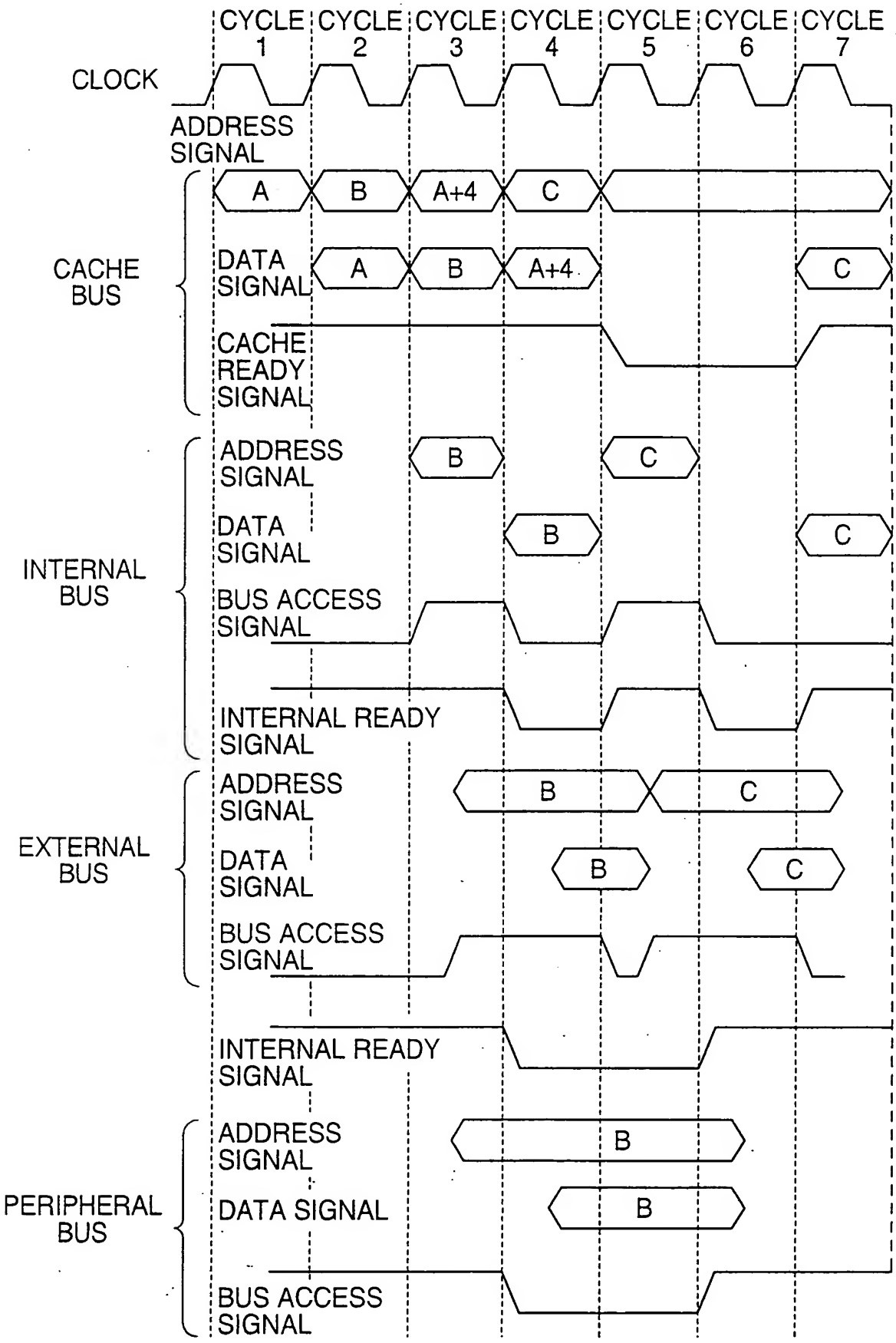

CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
CYCLE 5
CYCLE 6
CYCLE 7
CLOCK
ADDRESS SIGNAL
A
B
A+4
C
CACHE BUS
DATA SIGNAL
A
B
A+4
C
CACHE READY SIGNAL
INTERNAL BUS
ADDRESS SIGNAL
B
C
DATA SIGNAL
B
C
BUS ACCESS SIGNAL
INTERNAL READY SIGNAL
EXTERNAL BUS
ADDRESS SIGNAL
B
C
DATA SIGNAL
B
C
BUS ACCESS SIGNAL
INTERNAL READY SIGNAL
PERIPHERAL BUS
ADDRESS SIGNAL
B
DATA SIGNAL
B
BUS ACCESS SIGNAL

FIG. 33

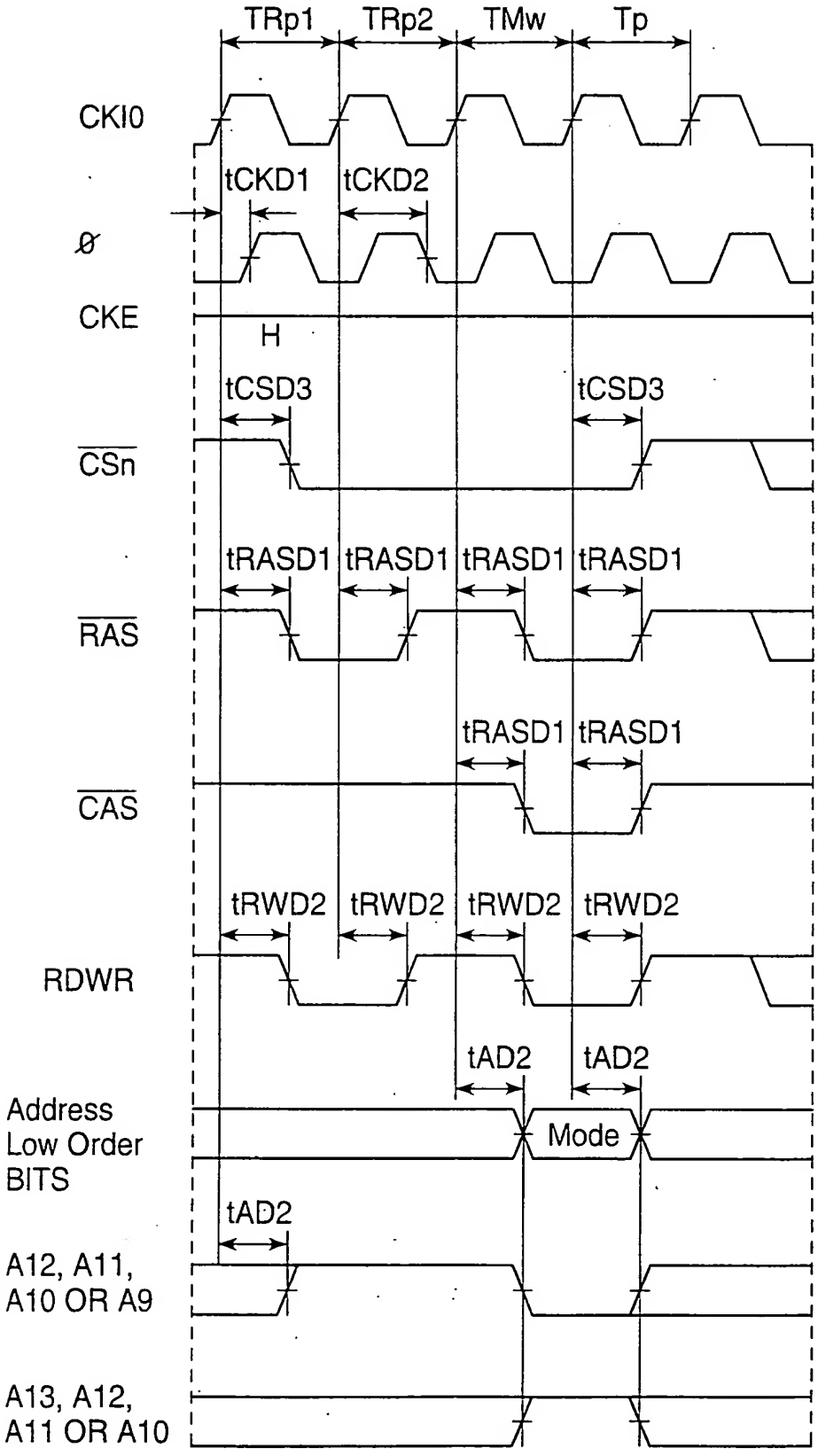
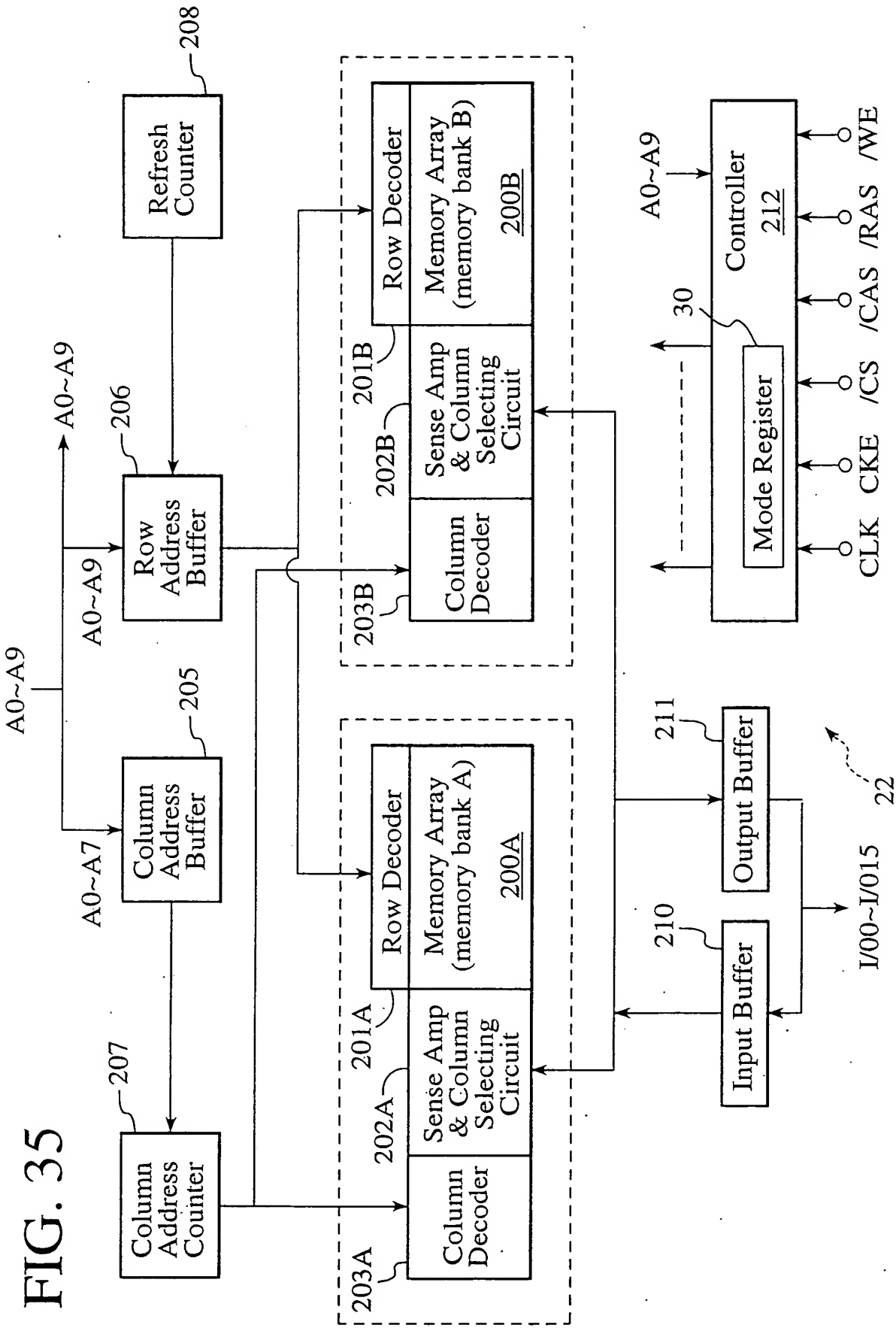

TRp1
TRp2
TMw
Tp
CKI0
tCKD1
tCKD2
ø
CKE
H
tCSD3
tCSD3
CSn
tRASD1
tRASD1
tRASD1
tRASD1
RAS
tRASD1
tRASD1
CAS
tRWD2
tRWD2
tRWD2
tRWD2
RDWR
tAD2
tAD2
Address
Low Order
BITS
Mode
tAD2
A12, A11,
A10 OR A9
A13, A12,
A11 OR A10

FIG. 34

FIG. 35


Refresh Counter
208
A0~A9
206
Row Address Buffer
A0~A9
A0~A9
205
Column Address Buffer
A0~A7
207
Column Address Counter
Row Decoder
Memory Array (memory bank B)
200B
201B
202B
Sense Amp & Column Selecting Circuit
203B
Column Decoder
Row Decoder
Memory Array (memory bank A)
200A
201A
202A
Sense Amp & Column Selecting Circuit
203A
Column Decoder
A0~A9
30
Controller
212
Mode Register
CLK
CKE
/CS
/CAS
/RAS
/WE
211
Output Buffer
210
Input Buffer
I/00~I/015
22

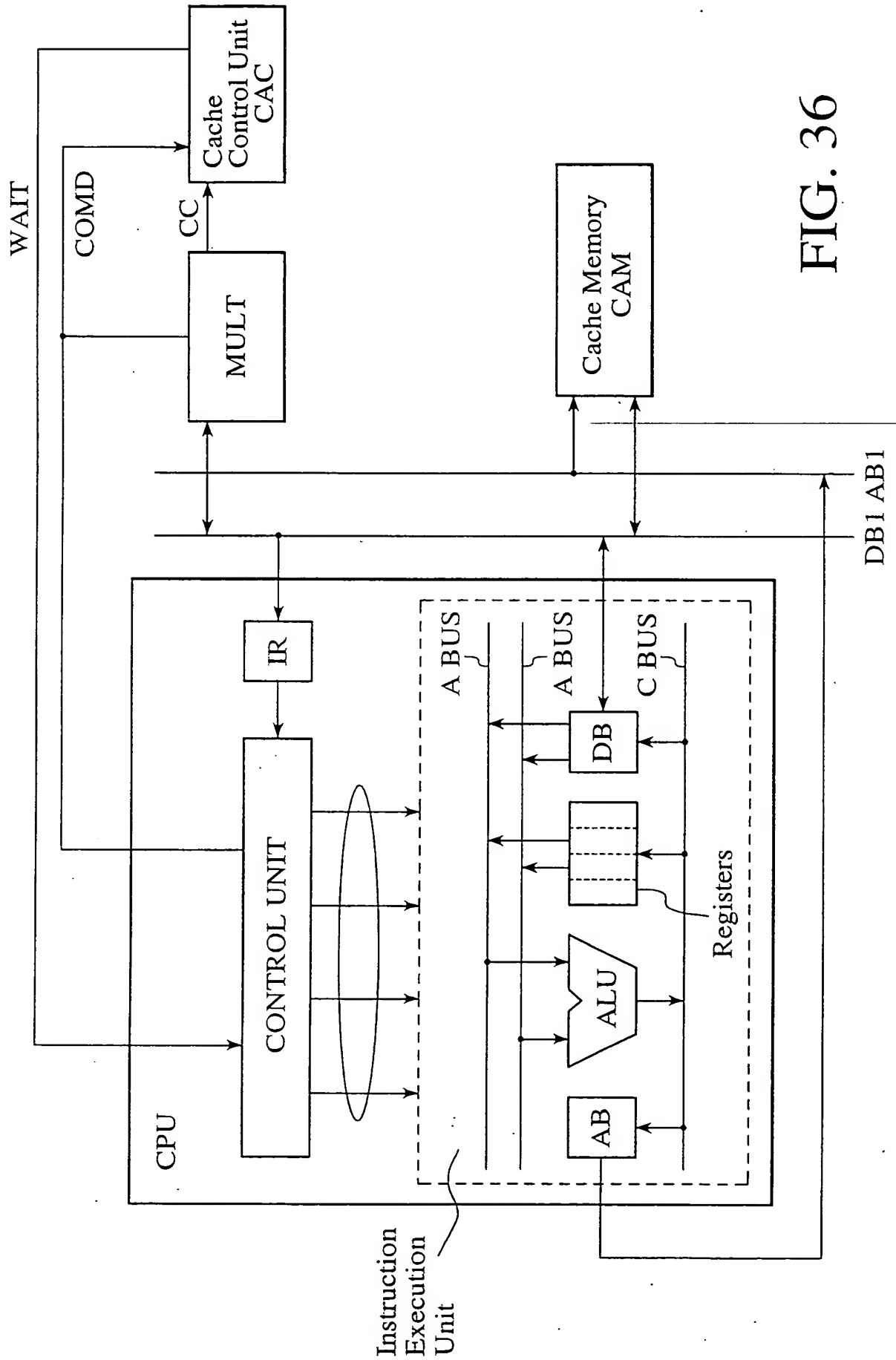

WAIT
COMD
CC
Cache Control Unit CAC
MULT
Cache Memory CAM
DB1 AB1
CPU
IR
CONTROL UNIT
A BUS
A BUS
C BUS
DB
ALU
AB
Registers
Instruction Execution Unit

FIG. 36

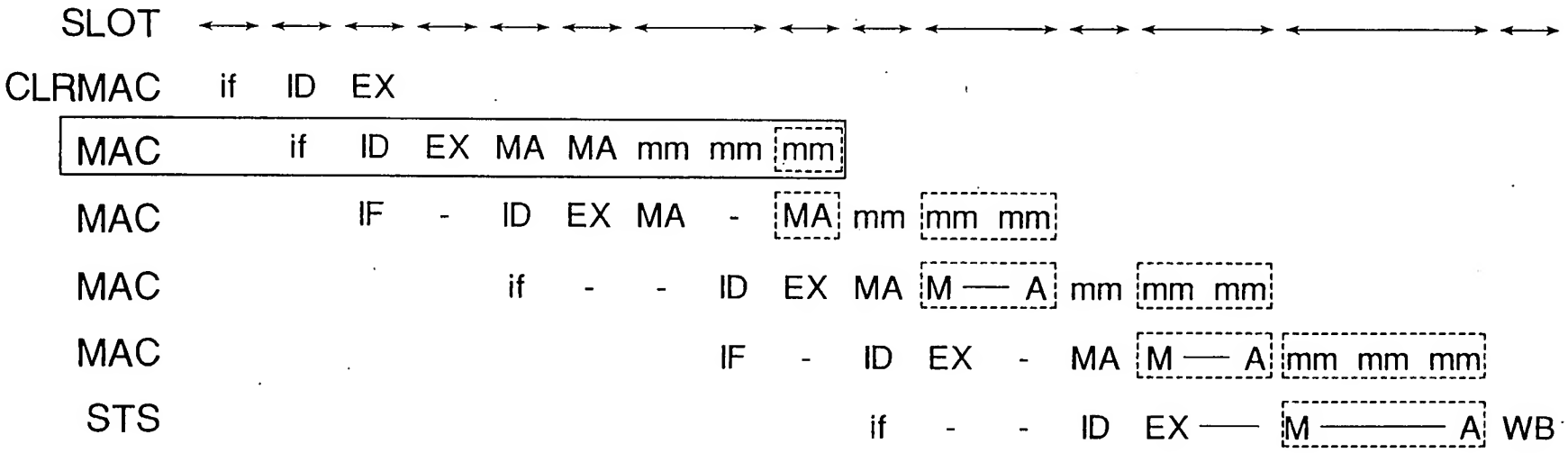

SLOT
CLRMAC if ID EX
MAC if ID EX MA MA mm mm mm
MAC IF - ID EX MA - MA mm mm mm
MAC if - - ID EX MA M — A mm mm mm
MAC IF - ID EX - MA M — A mm mm mm
STS if - - ID EX — M ——— A WB

FIG. 37

FIG. 38

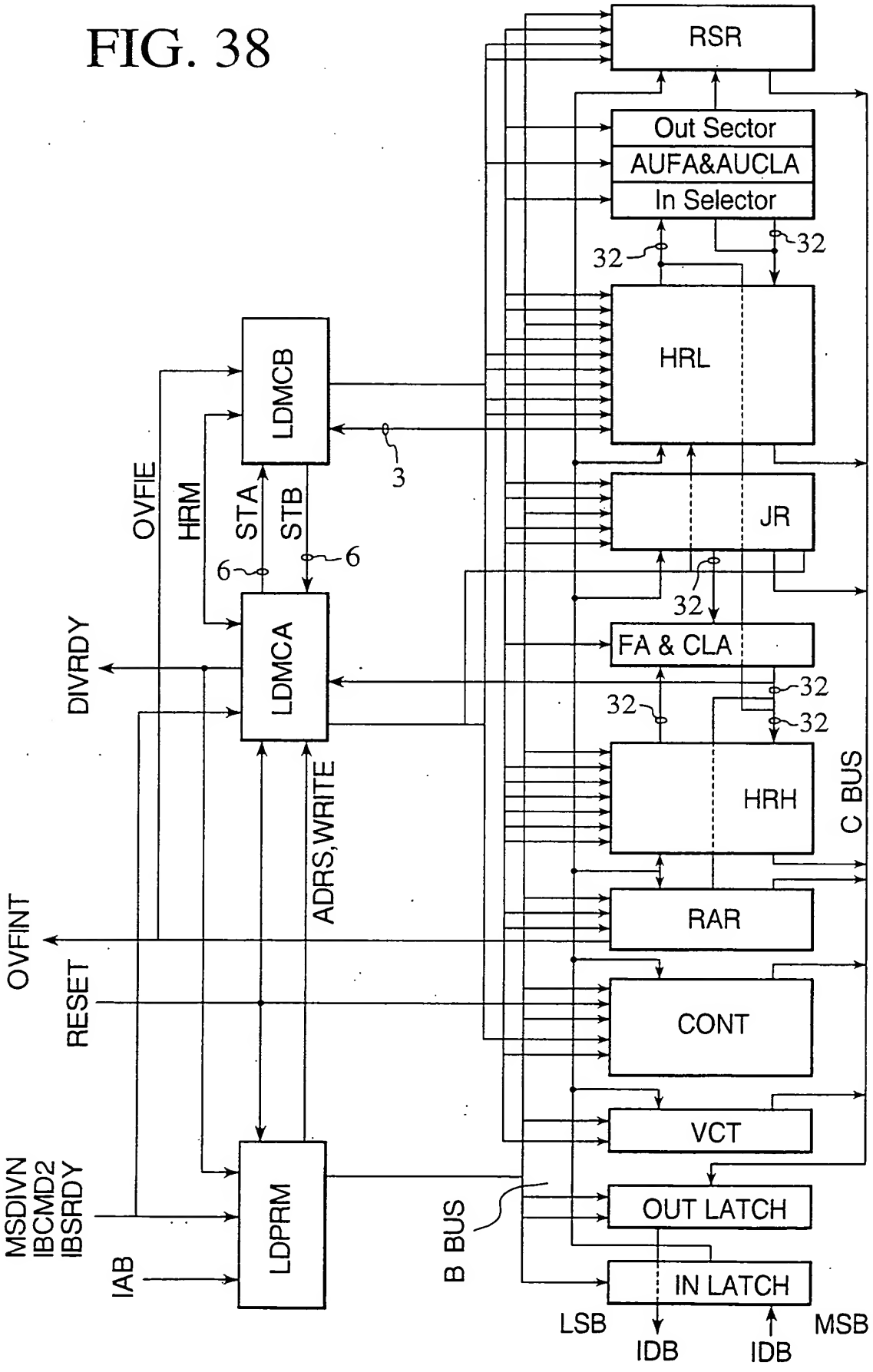

RSR
Out Sector
AUFA&AUCLA
In Selector
32
32
HRL
JR
32
FA & CLA
32
32
HRH
RAR
CONT
VCT
OUT LATCH
IN LATCH
LSB
MSB
IDB
IDB
C BUS
B BUS
LDMCB
LDMCA
LDPRM
3
6
6
STA
STB
HRM
OVFIE
DIVRDY
ADRS,WRITE
OVFINT
RESET
MSDIVN
IBCMD2
IBSRDY
IAB

FIG. 39

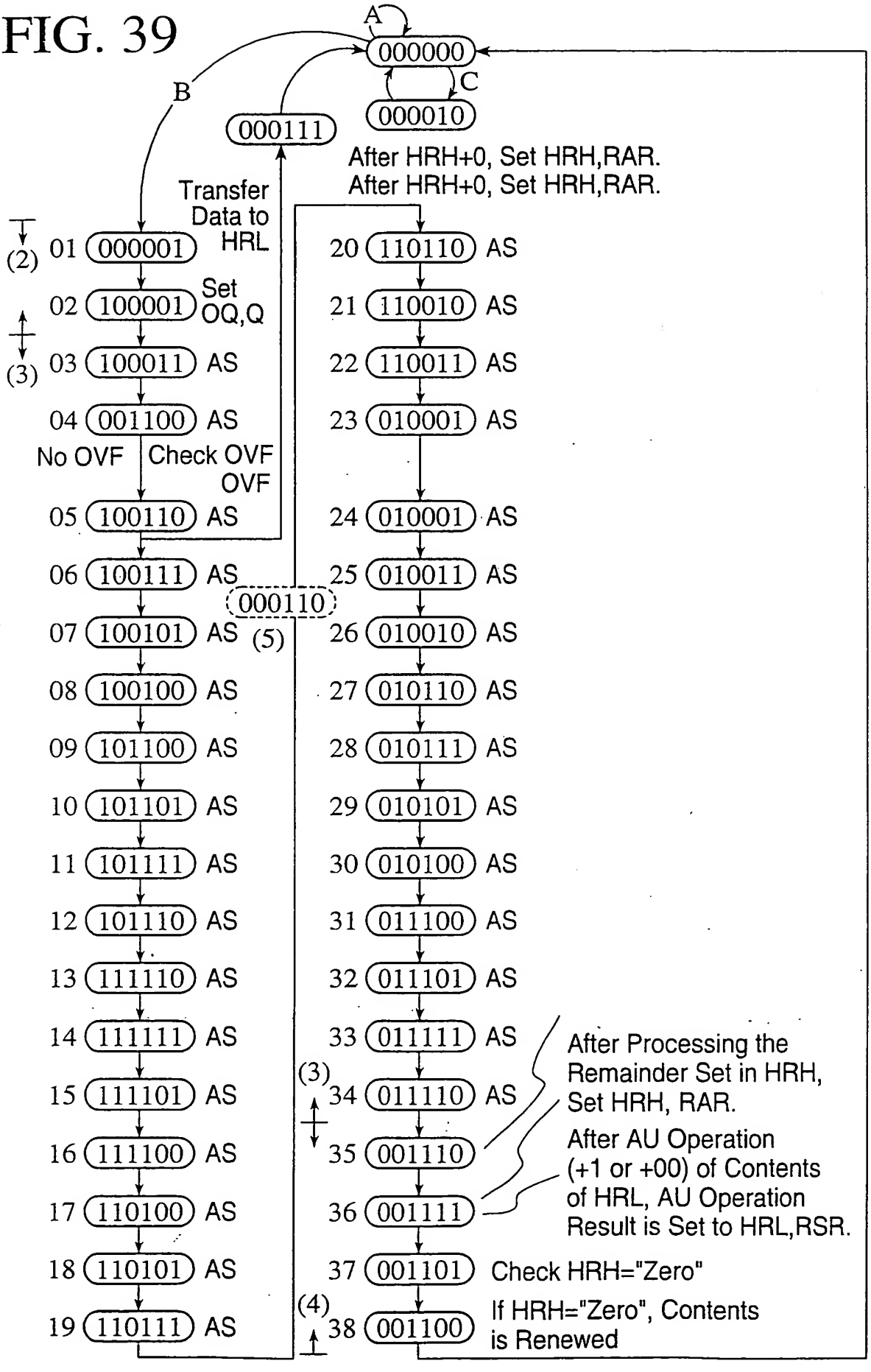
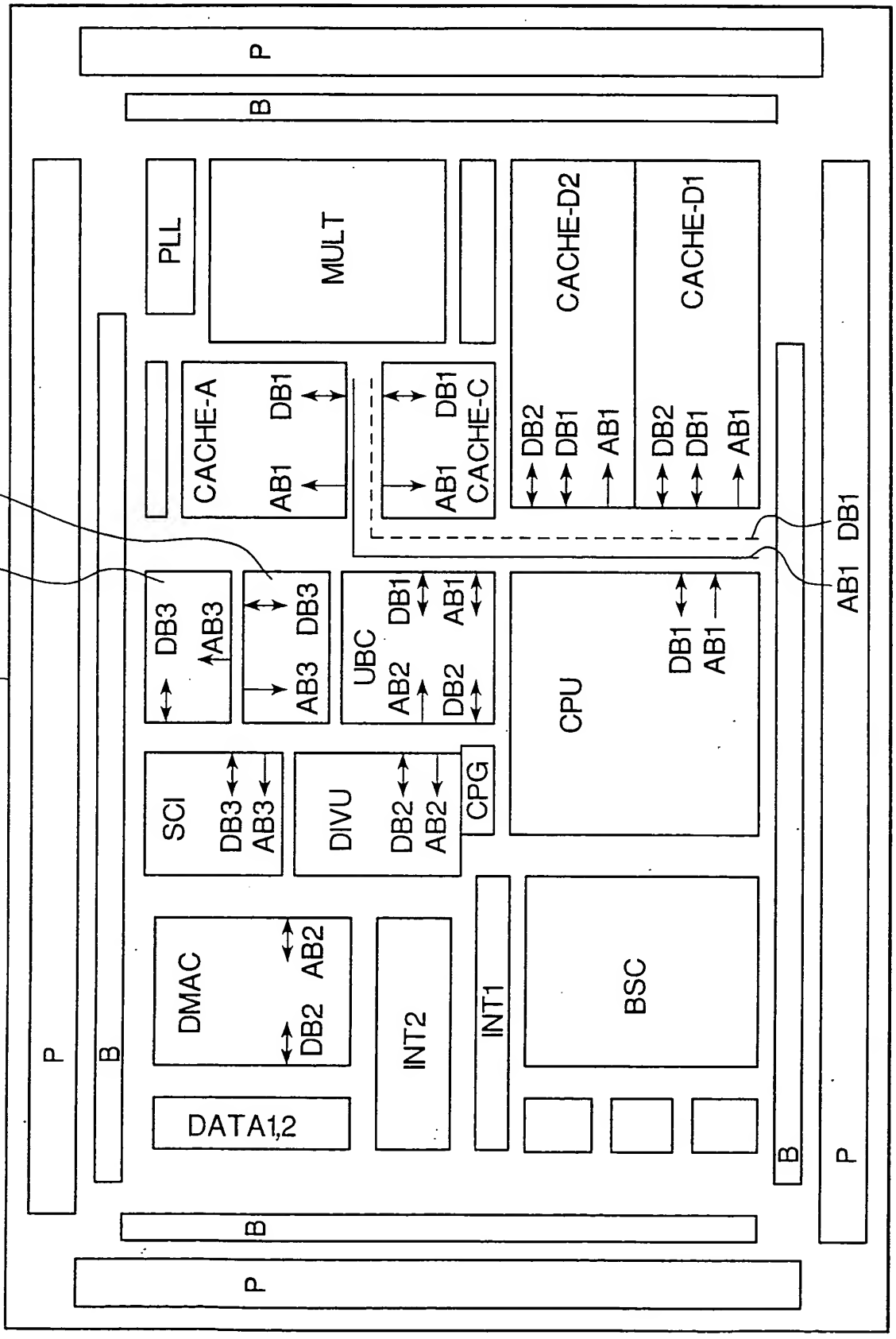

A
000000
B
C
000010
000111
After HRH+0, Set HRH,RAR.
After HRH+0, Set HRH,RAR.
Transfer Data to HRL
(2)
01 000001
02 100001
Set OQ,Q
(3)
03 100011 AS
04 001100 AS
No OVF
Check OVF
OVF
05 100110 AS
06 100111 AS
07 100101 AS
08 100100 AS
09 101100 AS
10 101101 AS
11 101111 AS
12 101110 AS
13 111110 AS
14 111111 AS
15 111101 AS
16 111100 AS
17 110100 AS
18 110101 AS
19 110111 AS
000110
(5)
20 110110 AS
21 110010 AS
22 110011 AS
23 010001 AS
24 010001 AS
25 010011 AS
26 010010 AS
27 010110 AS
28 010111 AS
29 010101 AS
30 010100 AS
31 011100 AS
32 011101 AS
33 011111 AS
(3)
34 011110 AS
35 001110
36 001111
37 001101
(4)
38 001100
After Processing the Remainder Set in HRH, Set HRH, RAR.
After AU Operation (+1 or +00) of Contents of HRL, AU Operation Result is Set to HRL,RSR.
Check HRH="Zero"
If HRH="Zero", Contents is Renewed

FIG. 40


Semiconductor Chip
FRT
WDT
P
B
PLL
MULT
CACHE-A
CACHE-C
CACHE-D2
CACHE-D1
DB1
AB1
DB2
AB2
DB3
AB3
UBC
CPU
SCI
DIVU
CPG
DMAC
DATA1,2
INT2
INT1
BSC

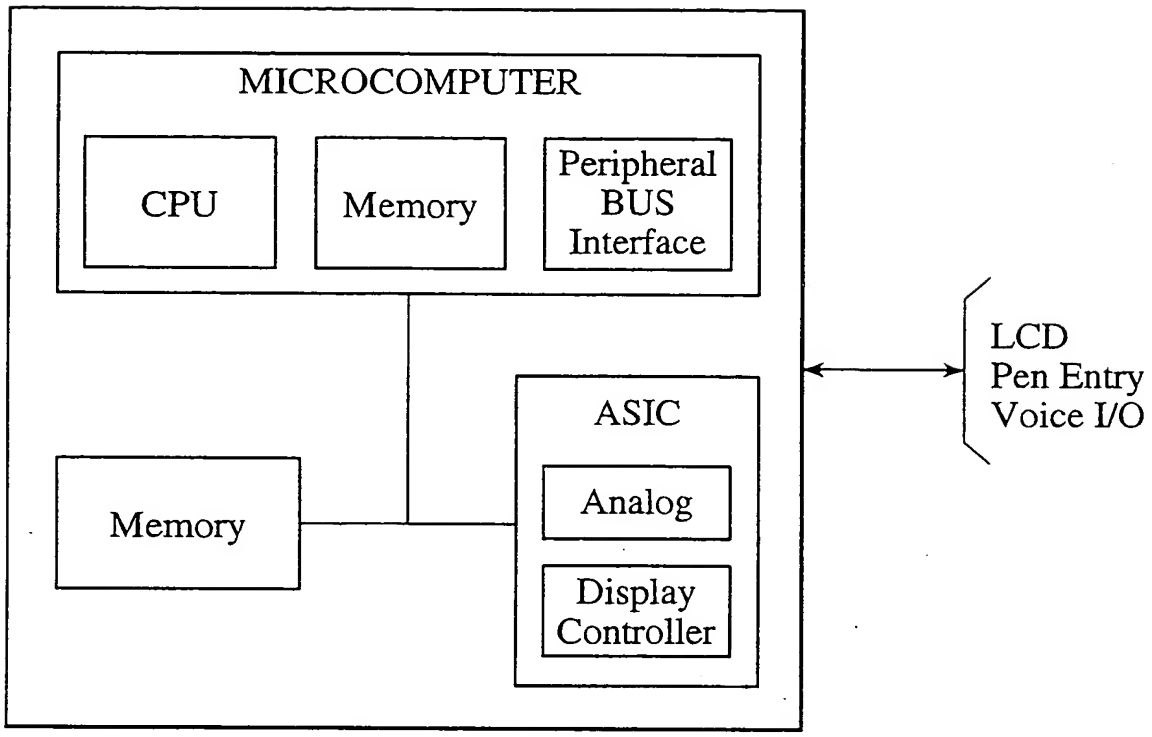


FIG. 41A

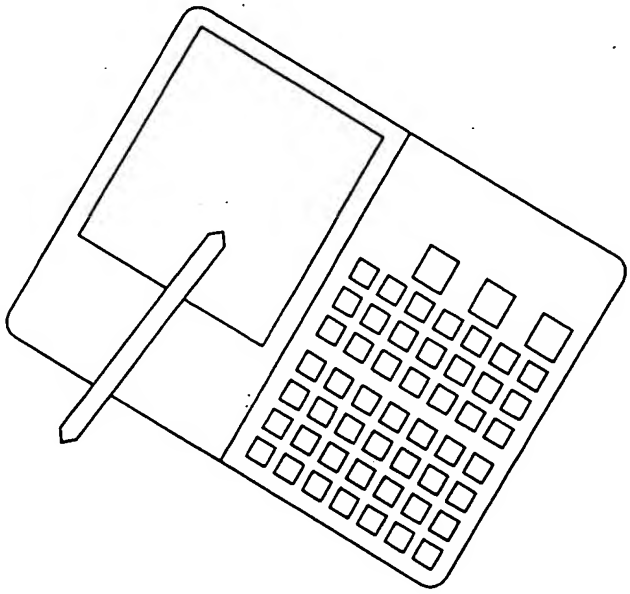
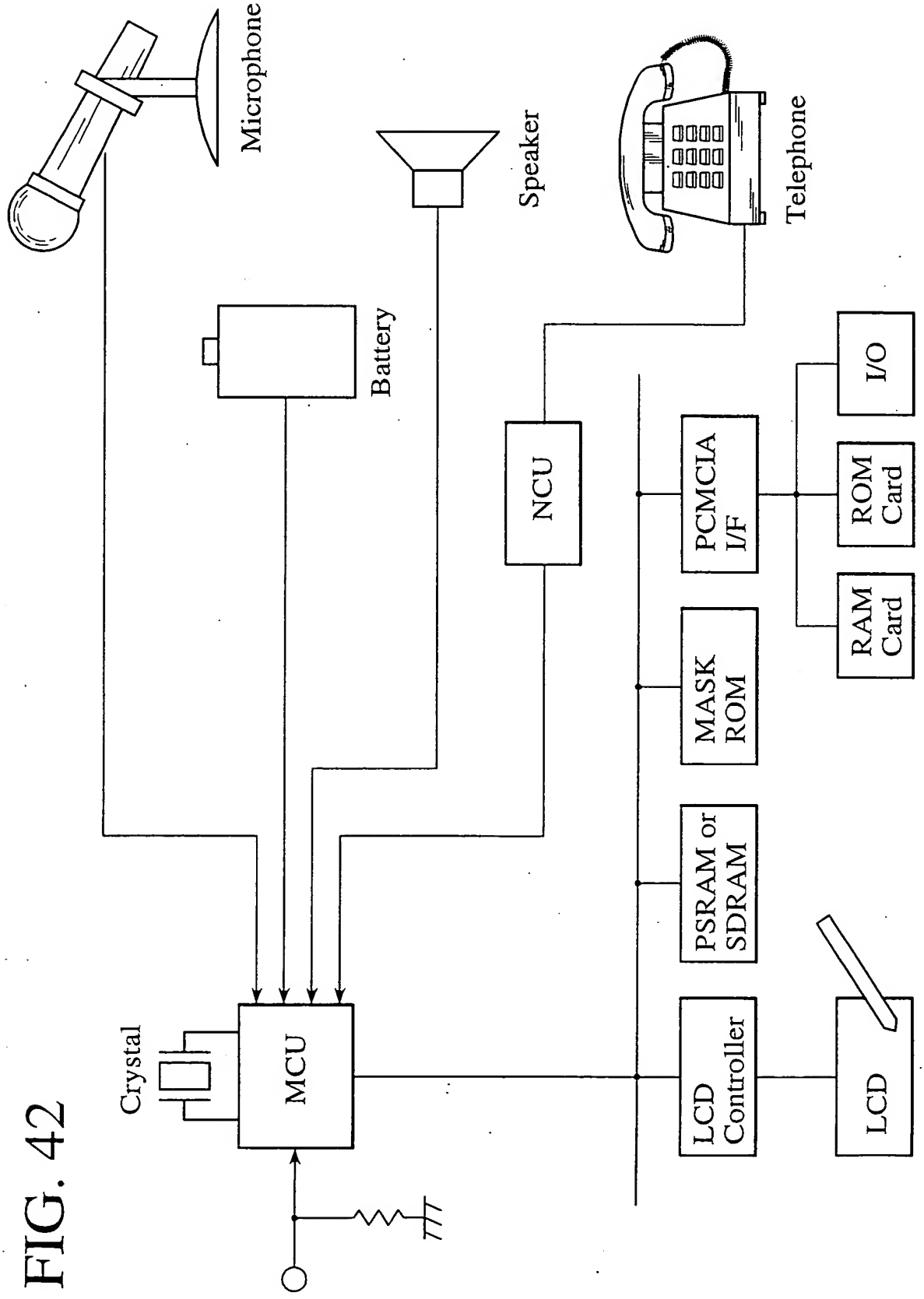


FIG. 41B

FIG. 42


Microphone
Speaker
Telephone
Battery
NCU
PCMCIA I/F
I/O
ROM Card
RAM Card
MASK ROM
PSRAM or SDRAM
LCD Controller
LCD
Crystal
MCU